PROTEUS

ADAPTIVE MICROFLUIDIC - AND NANO - ENABLED SMART SYSTEMS FOR WATER QUALITY SENSING

WP2-Smart Systems co-design and sub-part specifications

D2.2

Second version of smart system co-design

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Abstract

The outcome of the first functional prototype fabrication and test reported on deliverables D5.1 and D5.2 provided the guidelines and specifications for the design of the final version of the PNODE.

The final architecture of the second version of the PNODE with improved co-design of each sub-system is here detailed, including: **housing** and **support board**, **sensing chip**, **CMOS chip**, **communication system**, **software integration** and **energy harvesting**.

A brief summary of the PNODE status and validation carried out in laboratory and in the Sense-City platform is reported, then, each building block is here detailed. The main changes of the 2nd version address the limitations and integration issues encountered during the validation process of the 1st version: mechanical interface, sensitivity of the sensors chip, bonding, communication protocols, limited powering.

This deliverable is fundamental to conclude the WP2 and is necessary for the completion of fabrication, integration and testing (WP3, WP4) as well as the deployment and field test in the real environment of the PNODE (WP5).

Disclaimer

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V0.1	14/01/2017	Creation	Francesco Cottone (UNIPG)
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Executive summary

The objective of the WP2 work-package is the complete design of the PNODE. The first deliverable of the WP2 (D2.1) presented the preliminary design of the device on the basis of the operative requirements of the different use cases. The first version of the Pnode, which was tested both in laboratory and at the Sense-City facility (D5.1 and D5.2), was quite effective in answering to most of the requirements, but it also evidenced some limitations which had to be overcome in the subsequent design. Some of these limitations appeared already from the first test stages so that the devices tested in D5.1 and D5.2 deliverable show small changes with respect to the D2.1 design. Such changes are partly discussed in this deliverable together with the presentation of the final design

The major aim of this second version is the integration of all the components of the device. Regarding this aspect, the major changes are:

1. the integration of the electronics in a single CMOS chip, providing energy management and wireless capability in addition to the signal acquisition and elaboration, which was already carried on at the single chip level. Several versions of the chip are presented, showing the improvement of its onboard functionalities.
2. the integration on the MEMS platform, for which an enhanced fabrication process flow allows the full cointegration of all PROTEUS sensors on a single monolithic silicon chip, from chemical sensor based on CNT to physical ones, with particular care for the pressure sensor, whose fabrication requires a significant increase of the lithographic steps and for the flow sensor.

Moreover, significant improvements are present also in the design of the single subparts, where the limitations observed in the experimental test (see D5.2 conclusions) have been addressed:

a) Optimization of the control of CNT printing, for increased reproducibility and device density.

b) Optimization of the analog front end and digital processing unit.

c) Novel design of the water flux energy harvester for water speed below 1 m/s.

d) Optimization of the protective coating of the sensor cap.

1 Outcome of first version

1.1 Summary of features of first version

The first functional prototype has been provided in deliverable D5.1. It integrates the support board, the caps with sensing and CMOS chip, a piezoelectric energy harvesting system including power management circuit, the operational software with predictive algorithms as well of communication board. The main features of the first prototype are summarized as follows:

- **PNODE**: small-scale mechanical integration of all sensing and electronic components.
- **SENSING**: capsule board of 27 mm of diameter includes CNT and MEMS sensor chip together with a CMOS chip allowing measurements of pH, chlorine, chloride, conductivity, flowrate, pressure, temperature.
- **COMMUNICATION**: communication via Modbus library specifically designed to run on the PNODE with support of RS-485 (wired) or LoRa (wireless) communication infrastructures. Data coming for sensing capsule are acquired and sent to the PLC and production SCADA using the Modbus protocol. In addition, predictive Oracle software provide short term descriptions sent back to the PLC.
- **POWERING**: dual energy harvesting system (piezoelectric vortex generator from water flow and solar cell) has been integrated together with local PLC equipment.

1.2 Summary of validation results

The validation of the first prototype has been carried out through the laboratory and Sense-City measurement campaign. The details are described in D5.2. We report here a brief summary of them:

- Packaging
  - Up to 10 bars,
  - No mechanical failure: PCB in place, no degradation of the chips,
  - Encapsulation resist stable, but degradation of globtop exposing wirebonding.
- Sensing
  - Linear relationship between **temperature**, **conductivity**, pressure, **pH, active chlorine** and **chloride** and sensor output voltage,
  - Flowrate sensor: nonlinear decrease of resistance with flow rate.
- Electronics and communication
  - CMOS chip: successful Analog to digital conversion with simulated conductivity sensor.
  - Modbus over RS485 and Modbus over LORA communication to Water Management System
- Software
  - Oracle predictive software: successful prediction for reference sensors (error: less than 0.9%) and for the PNODE temperature sensor (error: 0.2%).
- Energy Harvesting
  - Piezoelectric generator characterized in water speed from 0.1 – 1 m/s. Power generated from 1µW at 0.4m/s to 50µW at 1.2m/s (to improve by 1 order of magnitude with 2nd version). Successful connexion as power supply for the the PNODE electronic card (V1.1).

To prepare the second and third run of Proteus, additional analysis and measurements both in the lab and in Sense-City could provide valuable additional inputs, notably regarding to the following topics:

- Sensing cap
  - Extended variation of conductivity sensors,
  - Chlorine level at higher pH,
  - Temperature in extended range,
  - Response time ,
- Communication
- Energy Harvesting,
  - Improved power density,
  - Capability to recharge battery,
  - Reliability.

1.3 Goals of second and third versions of design

The goals for optimization of the 2nd and 3rd version of PNODE are suggested by D5.2. The principal guidelines are listed in the following Table 1:

Table 1 – Design evolution from 1st version to 2nd and 3rd versions of PNODE.

PNODE version	1st version	2nd version	3rd version
Status	• Assembly done • Validation in progress	• Building blocks in finalization • Assembly second quarter 2017 • Validation third quarter 2017	• Building blocks started • Assembly and validation fourth quarter 2017
Sensing	• MEMS: temperature, pressure, flow rate, conductivity • CNT: 3x3 sensor array, pH, Chloride, Chlorine • 7 parameters on the same chip, up to 16 sensing elements	• MEMS: temperature, pressure, flow rate, conductivity • CNT: 3x3 sensor array with **improved fabrication process**, pH, Chloride, Chlorine, **hardness**	• MEMS: temperature, pressure, **flow rate with optimized design**, conductivity • CNT: **5x5** sensor array with **decreased footprint by sensor**, pH, Chloride, Chlorine, hardness, **nitrate**
Electronics	• CMOS chip version 1 (analog) • V1.2 board for digital parts and additional analog features	• CMOS chip **version 2 (analog & simple digital features)** • V1.2 board • **HW and SW level improvement of noise**	• CMOS chip **version 3 (improvedanalog & full digital)** • Minimal V2 board
Software	• Modbus over RS-485 (wired) or LoRa (wireless) • Data acquisition by commercial water management system (WMS) • Predictive capabilities on WMS side	• Data acquisition by commercial WMS • **Bidirectional communication protocol** to WMS • **Smart operational SW on PNODE** • Predictive capabilities on WMS & **PNODE**	• Data acquisition by commercial WMS • Bidirectional communication protocol to WMS • Smart operational SW on PNODE • Predictive capabilities on WMS & PNODE
Packaging	• Cylindrical, replaceable sensor cap with sensor chip and CMOS chip mounted on PCB • Cylindrical housing with electronic card and battery, connected to energy harvester and antenna • Insertion of sensor cap into saddle clamp on pipe	• Cylindrical, replaceable sensor cap with sensor chip and CMOS chip mounted on PCB **(newer design). Optimized coating strategy** • Cylindrical housing with electronic card and battery, connected to energy harvester and antenna • Insertion of sensor cap into saddle clamp on pipe	• Continuous improvement in coating strategy • Drastically **reduced length of housing for** electronic card.
Energy harvester	• Dual energy harvesting: solar cell and piezoelectric vortex generator	• Two additional options for water flux energy harvesting: electromagnetic vortex generator and micro turbine	• Choice of material optimization

1.4 Details on Proteus subpart versions

Several versions of the PNODE hardware subparts were produced and are detailed in the following tables, for a better understanding of subsequent designs information:

Table 2 – Support board status

Versions	Description	AFE	Digital Part	Caps Compatibility
V1.1	Energy Harvesting Board!	None	MSP Commercial	None
V1.2	Without FPGA			
V1.2_FPGA	With FPGA for digital Part	All working, but Flowrate need hardwired resistor	External (Serial and I2C connection)	Caps V1
V1.2_Only_AFE	Digital part cuttout			
Digital_Lora_only_V1	Only Digital Part and Regulators	None	MSP Commercial	None

Versions	Energy Harverstor	Energy Needs	Energy Supply	Communication	Availabity
V1.1	Piezo, PV Cell, Battery and VCC 12-20V		3.3V		3
V1.2				None	5
V1.2_FPGA		3.3V		LORA RFM95W	5+4(waiting to arrive from external supplier)
V1.2_Only_AFE	None	3.3V + 0.9V		None	6 To Be Frabricated
Digital_Lora_only_V1	None	12V or 3.4V		LORA + RS485	6 To Be Frabricated

Table 3 – CMOS chip status

CMOS chip								
Versions	**Supported functionalities**	**Chip size**	**Number of chips by wafer**	Process yield	**Sigma Delta Modulation Analog Digital Converter**	**Amplifiers and Signal Conditioning**		**Cost in pre-series**
V1	Analog to digital converter, programmable gain input sample and hold, a programmable filter, a programmable analog MUX and a DC-DC converter (part of the power management unit). Interface 9 CNT chemical sensors and 7 MEMS physical sensors.	1.5mmx1.5mm	More than 45 CMOS IC dies were delivered. Some of them were partially isolated due to wire-bonding fine tunning.	The 130nm CMOS technology-higher than 90%.	The designed Sigma-Delta Modulator Analog to Digital Converter (SMD-ADC) has a peak Signal to Noise Ratio (SNDR) of 63.5 dB, a power consumption of just 5.86 µW for an input signal bandwidth up to 20kHz. The power supply voltage is 0.9V. For lower bandwidths, e.g. to interface with DC type sensors, the ADC can be dynamically adapted to achieve higher SNDR and lower power consumption and therefore reducing even further the energy per conversion step. Expected power usage per conversion is between 40 fJ and 150 fJ, depending on the required resolution and input bandwidth.	The programmable gain sample and hold and programmable filter have power consumption < 450 µW with 0.9 V power supply		Cost per sample to 260€, well below the target value.
V2.1	added digital part including the microcontroller and dedicated digital signal processing units and short-range wireless communication capability	1.5mmx1.5mm	It is expected to receive the same quantity. However a second chip was also be sent for fabrication which will guarantee the double of dies.	same high level of process yield	Same performance is expected.	Gain accuracy has been improved by design.		
V2.2	added digital part including the microcontroller and dedicated digital signal processing units and short-range wireless communication capability		In the MPW run a mimum of 50 will be received. For this type of run it is possible to order more die units	same high level of process yield	Same performance is expected.	The input impedance has to be increased, in accordance with the baseline resistance of some sensors.		The 5x5mm2 will cost aprox. 30kEuros, for a minimum of 50 dies.

Table 4 – Sensor Chip status

Sensor Chip								
Versions	Description	Conductivity	Temperature	Pressure	Flowrate	PH CL- CL2	Hardness	Nitrate
V1.2 Type 1		Non Linear Behaviour	Same	The ones with Square sensor are tested in the lab, the other is not tested	Not worth to test at this stage (Higher flowrate and high power consumption 10mW)	Tested		
V1.2 Type 2								
V1.2 Type 3								
V2.1	Same MEMS Chip as V1.2						Yes	
V2.2	Size and geometry of electrodes for CNT sensors will change to enable a larger number of CNT sensors				Next Generation Sensor	V2 (Updated Process)	Yes	Yes

Table 5 – Sensor caps version.

Caps PCB			
Versions	**Description**	**CMOS**	**Sensor Chip**
V1		PROTEUS1-3	V1, Type 1, 2 and 3
V1.1	Produced	PROTEUS1-3	V1, Type 1, 2 and 3
V2	Flex PCB	PROTEUS4	

Table 6 – Energy Harvesting System

Energy Harvesting System				
Versions	**Description**	**Energy source**	**Power level**	**Technology**
V1	Piezoelectric Generator based on Von Karman Vortex	Water flow	10 - 100 uW	Piezoelectric
	mini PV cell	Solar	10 - 100 mW	Photovoltaic
V2.1	Electromagnetic Generator based on Von Karman Vortex	Water flow	1 - 10 mW	Electromagnetic induction
V2.2	Micro Hydro Turbine	Water flow	1 - 20 mW	Electromagnetic

2 New PNODE design

The first version of the PNODE was based on a mixed configuration in which the most relevant analog signal acquisition, conditioning and digitalization steps are done, total or partially inside the CMOS chip and the remaining digital processing is performed by an external MCU installed in dedicated Support PCB board.

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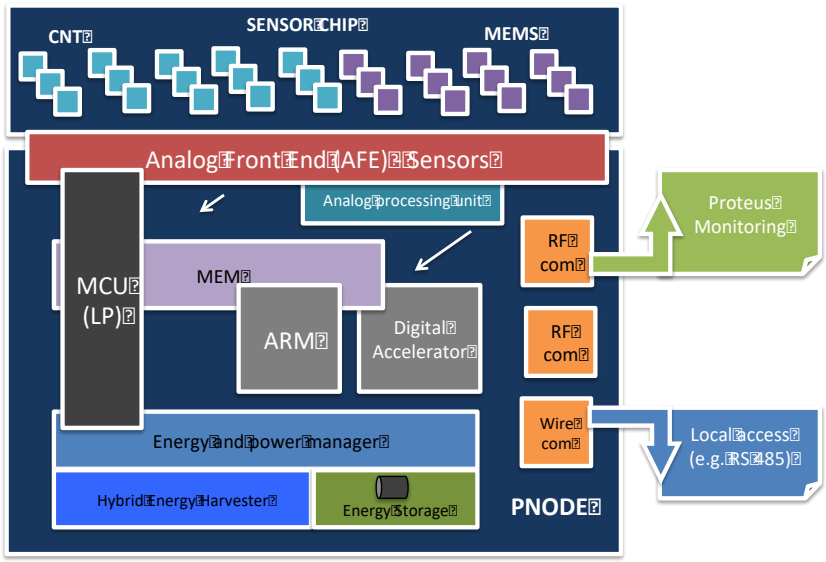


Figure 1: General system overview of the PNODE.

The later also provides wireless communications capabilities (short and long range), energy storage and interface circuitry for the hybrid energy harvester. A support PCB board is thus to be designed to connect the CMOS and Sensor chips.

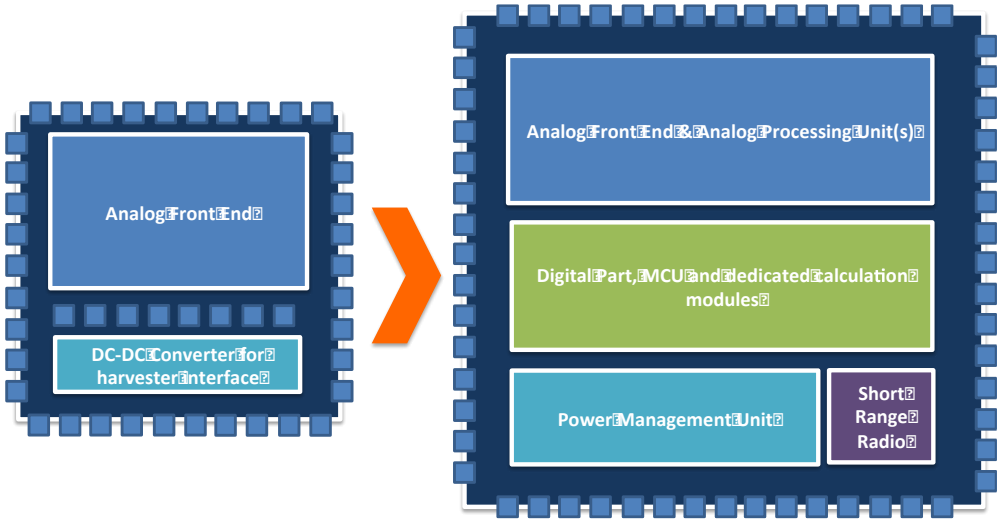


Figure 2: Evolution from first version to second version of the CMOS chip SoC.

Based on these considerations, the proposed block diagram of the first PNODE version is shown in Figure 3. A Printed Circuit Board (PCB) connects to the capsule board. The latter provides the connectivity between the Sensor Chip and the CMOS Chip.

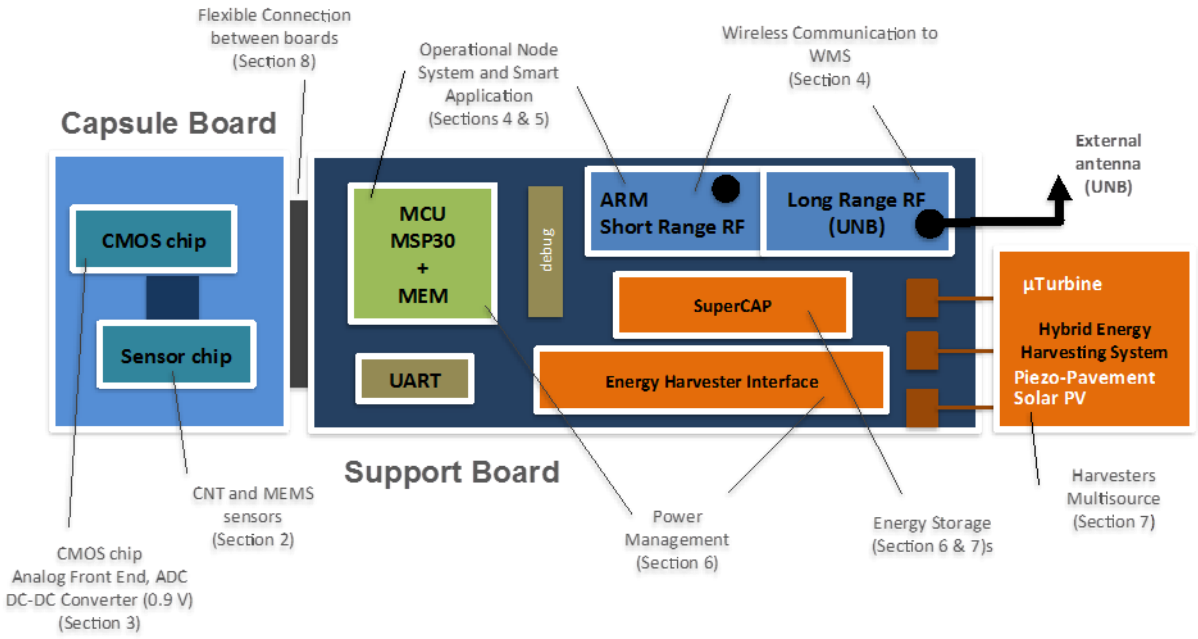


Figure 3: First Version of the electronic board: CMOS chip and sensor chip assembled into a capsule board, itself connected to a support board.

3 Support Boards

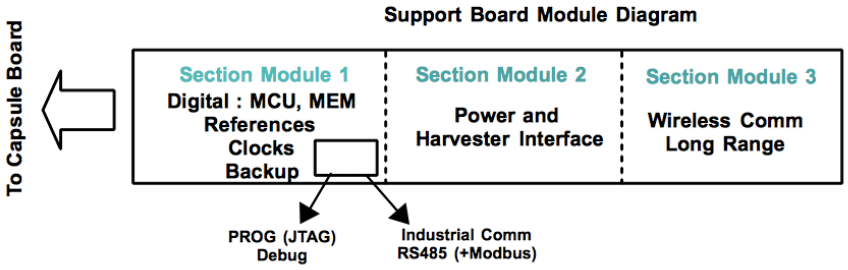
3.1 Board v1.1

The architecture of the board is divided in three Section Modules (See details in D3.3). The Section Module 1 includes the digital part to run the PROTEUS software (both operation and smart APP) and to generate supporting digital control/clock signals the CMOS chip. Besides this function this first section module include:

- A serial port interface that can be connected to a RS485 network driver circuit. Also available is the interface needed for the node program loading and debugging;
- Local Voltage regulators of 3.3 V, 1.2 V and 0.9 V (for the CMOS chip);
- Reference and clock generation circuits;
- An IC chip with an ARM processor and a Bluetooth Low Energy (BLE) transceiver. This latter emulates a short-range type of digital radio transceivers.

The Section Module 2, the power converter, interface with two types of energy harvesters, namely, a piezoelectric based harvester and a photovoltaic (PV) cell. An external battery can also be connected.

Finally, the third Section Module is responsible for the long range digital radio communications. It communicates internally with the microcontroller existent in section Module 1, via a serial link. In terms of radio communications, it uses an Ultra Narrow Band (UNB) transceiver. This radio digital technology significantly improve the sensitivity of the receiver and therefore increasing the coverage range.



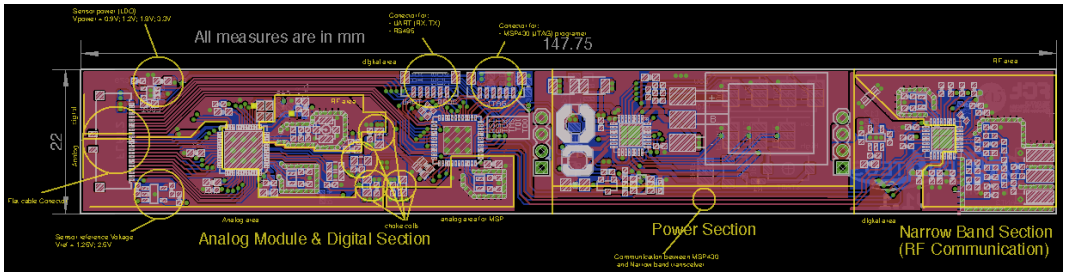


Figure 4 : Support Board V1.1.

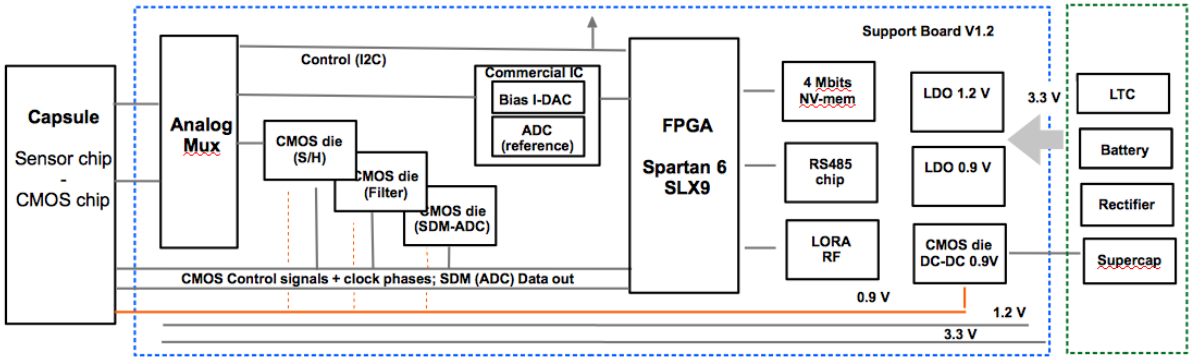
- A serial port interface that can be connected to a RS485 network driver circuit. Also available is the interface needed for the node program loading and debugging;
- Local Voltage regulators of 3.3 V, 1.2 V and 0.9 V (for the CMOS chip);
- Reference and clock generation circuits;
- An IC chip with an ARM processor and a Bluetooth Low Energy (BLE) transceiver. This latter emulates a short-range type of digital radio transceivers.

Two units have been assembled and positively tested both electrically and with software deployed with the Code Composer.

3.2 Board v1.2

A second version of the support board, designated by V1.2, was developed with an update of the connectivity layout to the capsule board and including a FPGA synthesised MSP 430 (replacing the commercial MSP430 from TI) (See details in D3.3). This constitutes an intermediate step which is closer to the final configuration intended for the CMOS chip second version. Moreover, additional improvements were included/modified:

- Radio section has been updated to be LORA compatible. A module is directly attached at the bottom of the board. This facilitates the replacement by other type of communication standard.
- A set of analog multiplexers have been added to select individual lines from the capsule board, enabling the route of the Sensor chip and CMOS chip signals to the support board. Since that after gluing and encapsulating the capsule board, the chips terminals are no longer directly accessible, this new configuration of the support board gives much more flexibility during the testing phase. In addition to this, extra CMOS chips dies (up to 3) can be added to V1.2 support board, reinforcing (or even replacing, in case of failure) the one included in the capsule.
- An RS885 chip interface has been added to the board
- A non-volatile memory of 4 Mbit has been added, enabling the storage of more acquired sensor data
- The PROTEUS CMOS DC-DC 0.9 V converter has been added after successful tests performed with the external power module
- A commercial chip integrating a current Digital-to-Analog Converter (DAC) capable of delivering a sink/source up to 2 mA (e.g., to support the biasing of temperature sensor) is added. This chip also provides a high resolution Analog-to-Digital Converter (ADC) which will be used as a reference during the characterization and testing phase of the PNODE system. This facilitates the process, reducing the number of external calibration equipment needed.
- Several additional testing points were included to facilitate the testing phase. Also, a digital control interface for the AFE part, via I2C, was included enabling to bypass the FPGA and control the AFE from an external MSP430 microcontroller.



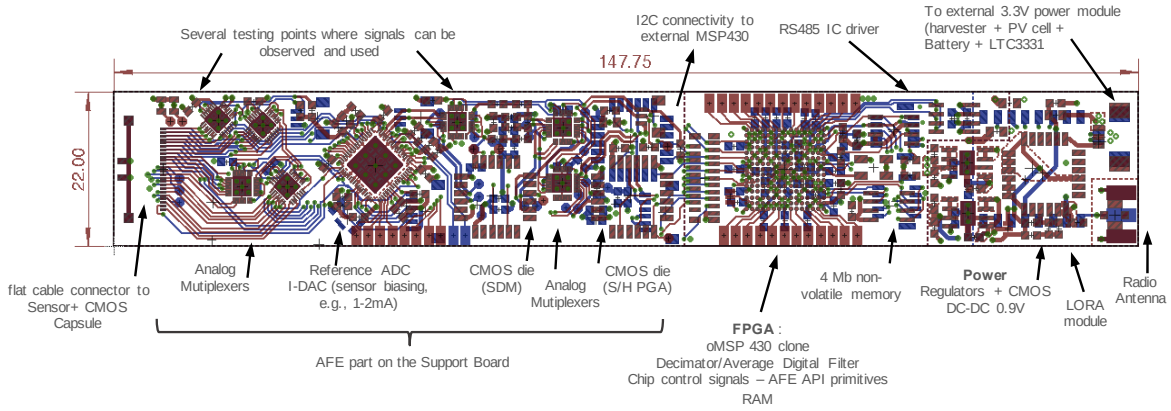


Figure 5 : Support Board v1.2.

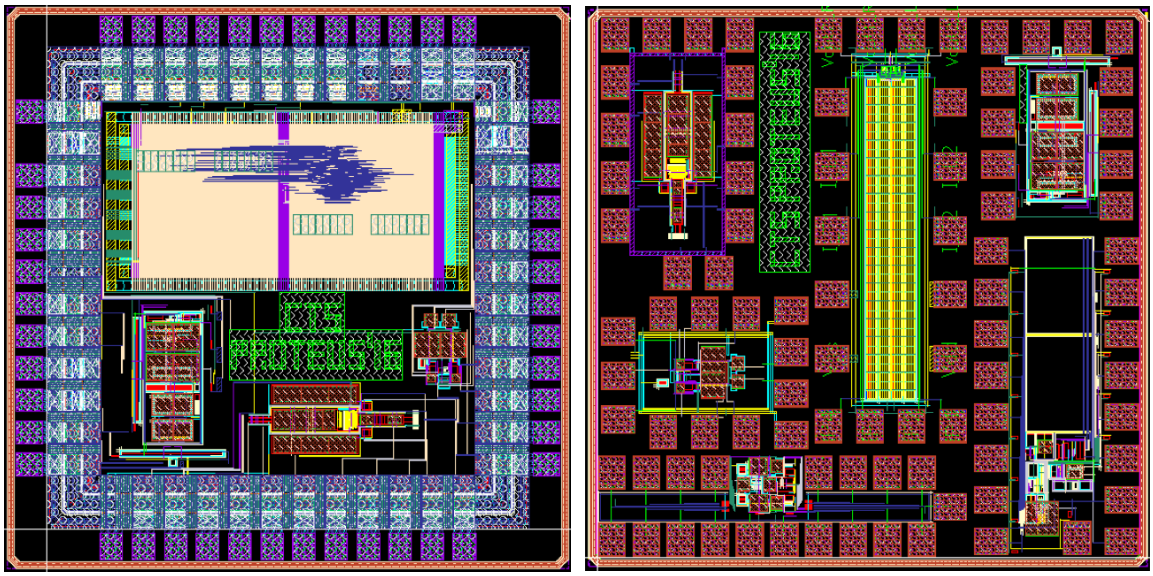
4 CMOS Chips

4.1 PROTEUS 1st run

First version, PROTEUS1, is described in D2.1 and D3.3.

4.2 PROTEUS 2nd run

Two chips were sent for fabrication in the November 2016 tapeout UMC CMOS 130 nm, **Proteus2** and **Proteus3**. Both ICs have an area size of 1.5 mm x 1.5m.



Proteus2 IC Proteus3 IC

Figure 6 : PROTEUS2 and PROTEUS2 chip layout..

4.2.1 Chip PROTEUS 2

Proteus2 is a mixed mode IC which includes a digital part and some of the most important building blocks of the AFE. The Digital part includes a MSP core, 4kB RAM memory for the program and 1kB RAM memory for Data. The analog part includes a SDM(ADC), programmable filter and a programmable gain S/H amplifier.

Proteus2 does not represent the final configuration of the final chip, namely at the memory level. It is intended to implement a 64kB RAM in the final chip version and follow a multicore approach, with two oMSP430 cores. It is not predicted to increase further this internal chip memory. Therefore, additional storage capacity (for example to save one day of sensor data) has to be guaranteed by an external Non-Volatile memory[1].

[1] http://www.macronix.com/en-us/products/NOR-Flash/Pages/Ultra-Low-Power-Flash.aspx
http://www.microchip.com/design-centers/memory
http://www.adestotech.com/products/enhanced-serial-flash/

Despite of its size limitations, the oMSP430 included in **Proteus2** can be used to run part of the code developed in PROTEUS project and to test the peripheral interface. This chip, in conjunction with the external FGPA,

- can be used to test the behaviour of the second MSP430 through the UART (RX-TX, program-debug) interface and running Proteus selected software routines.
- Controlling one analog peripheral, namely the SDM(ADC).
- Characterize the cpu enable control signal
- Obtaining power consumption profile relatively to the master clock
- Obtaining power consumption profile relatively to the power supply VDD

4.2.2 Chip PROTEUS 3

Proteus3 includes several analog building blocks for the AFE, including filter, SDM(ADC), quadrature oscillator, Integrator and Fire module and a DC-DC converter.

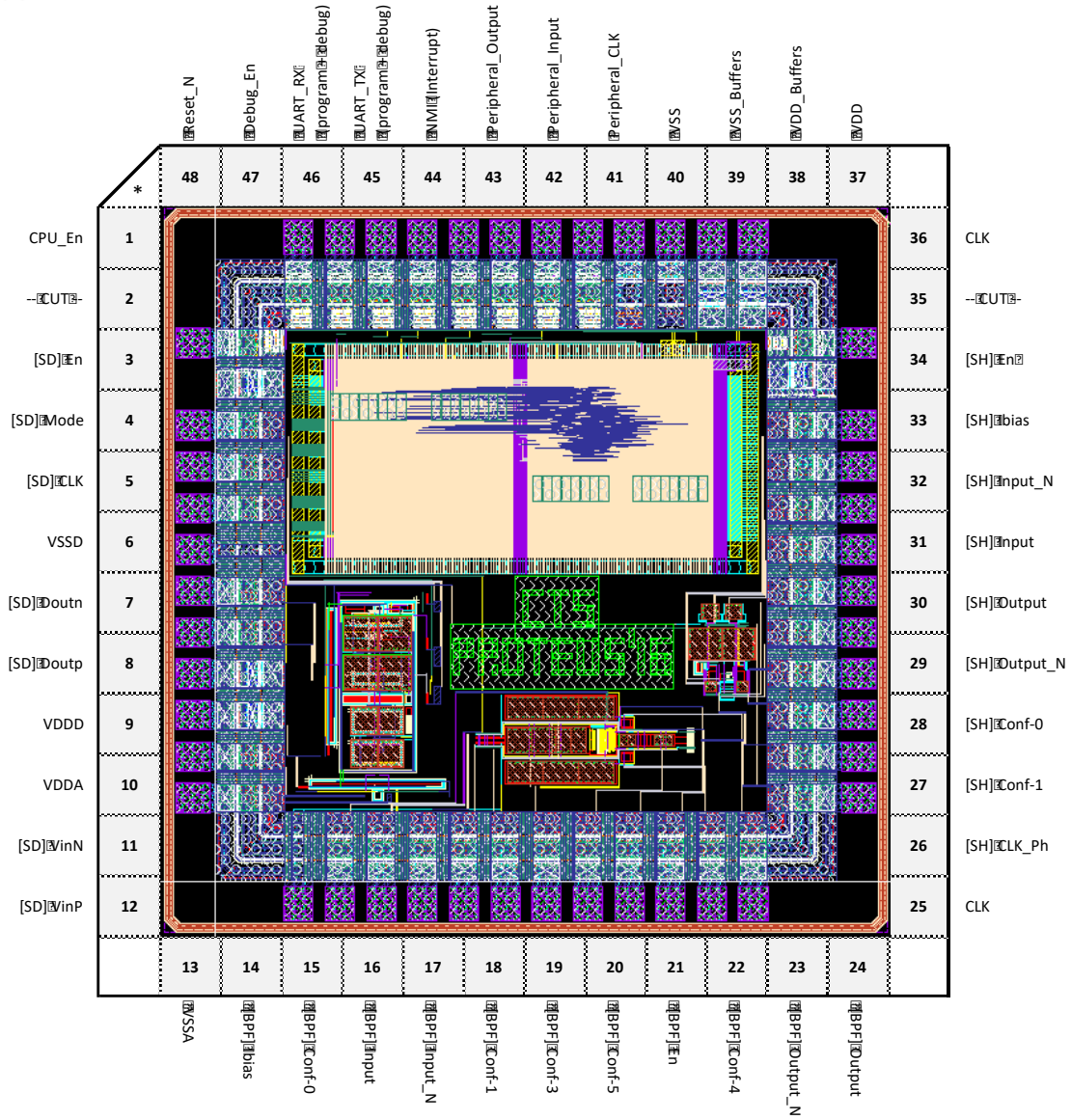


Figure 7 : Chip floorplan for Proteus 3 with detailed pad ring description.

4.3 PROTEUS 3rd run

4.3.1 Chip PROTEUS 4

Figure 8 shows the preliminary chip block diagram of PROTEUS4 IC. The total chip area is limited to a maximum of 25 mm^2 while keeping the total number of pads below or equal to 120.

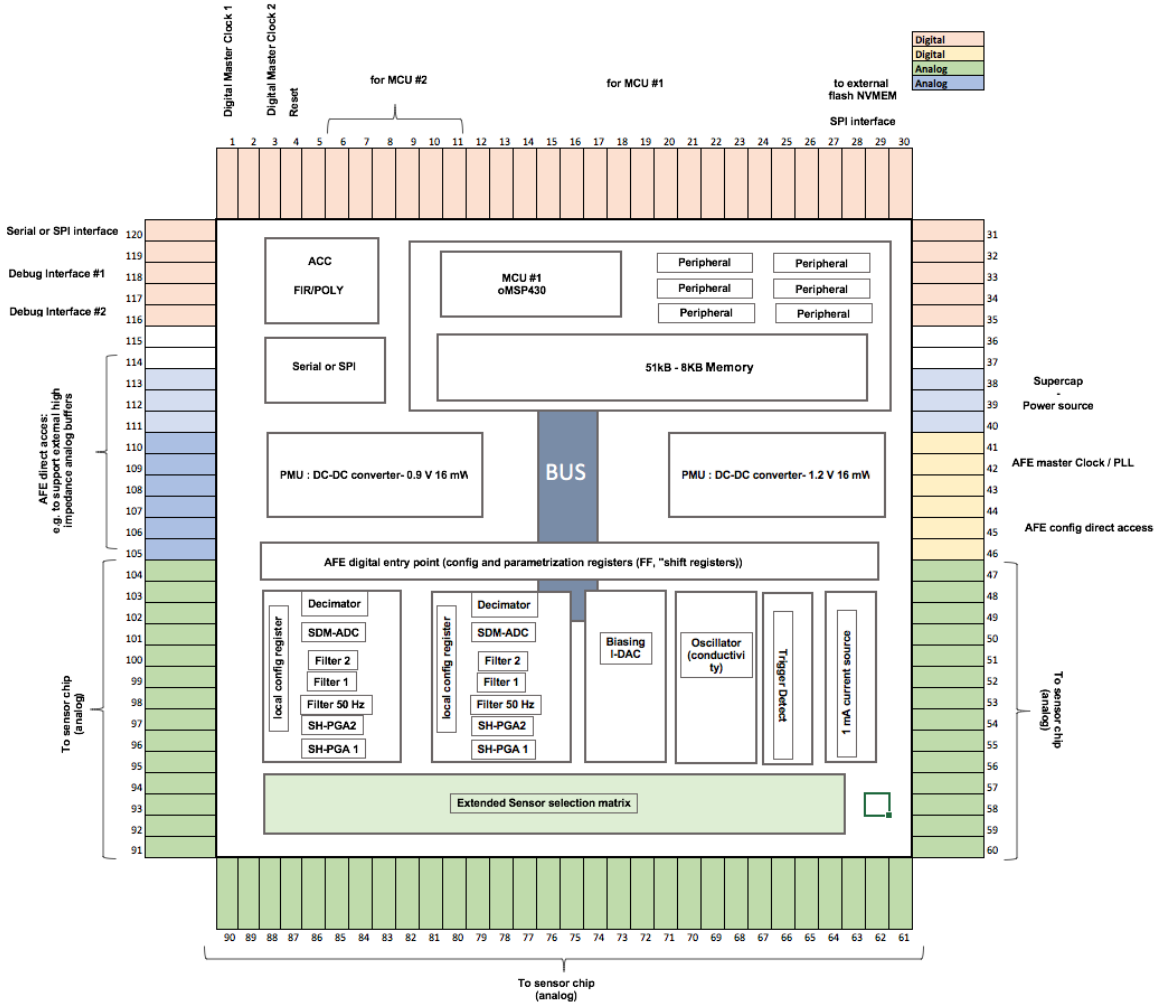


Figure 8 : Chip floorplan approach for PROTEUS4 .

The diagram represents a system on chip (SoC) where the placement of each building block depends on the nature of its processing functionality: digital or analog mixed-mode. It is a common approach to separate the analog part from the digital one. One of the reasons is to reduce the digital clock feedthrough effect though the substrate coupling. The digital area is located at the top while the analog one is at the bottom. Between them the power management unit is inserted not only to facilitate the power distribution but also imposing a wider separation between digital and analog areas.

General overview:

- Technology: 130 nm standard CMOS technology; nominal voltage of 1.2V.
- Power supply
    - DC-DC converter capable of converter an input voltage, between 0.7 to 2.2V, to a stabilized voltage of 0.9V. A 1.2V is also available for the digital part. The connection to an AC energy harvester implies the use of an external rectifier (full-wave, preferably). The maximum

output power is 16 mW. However, this level can be duplicated easily, at a cost of doubling the silicon area.
    - A 1.2V supply is also available for the digital part.
    - Several grounds and power voltage supply pads will be included in the pad ring, not only to bias the pad ring itself but also to power-up external components. However, since the external chips, usually, use a higher supply voltage it should be considered to add an external DC-DC for higher voltages, e.g., 3.3V. External chips: LORA module, RS485 driver and battery charger
    - Power management will be performed by the PMU unit and by the software running in the MCUs.
- Digital part is responsible for
    - High level digital signal processing
    - Data communication to an external recipient through a serial connection
    - Running the operational node software
- Analog part is responsible to
    - Sensor selection,
    - Sensor biasing
    - Signal acquisition and conditioning
    - Maintain two acquisition channels operational
- Timing:
    - The reference clock for the digital part is obtained externally
    - The reference clocks for the analog part are obtained externally from a PLL synthesizer

Digital Part

The Digital part includes one or two MCU, RAM, digital modules for SPI or serial for data communications and interface with an external flash memory. Additionally, a small set of logic functions are directly synthesised in CMOS and constitutes efficient modules both in speed and power consumption (when compared with 100% software based approach)

- MCU
    - Objectives: execute and/or integrate
    - Operational PNODE code (state machine)
    - Interface to the AFE, “mounting” them as peripherals
    - Interface with the data communication module via serial port or SPI
    - Execute the bootloader code
    - Low power consumption, meaning that it can run at a lower speed
    - Core: openMSP core
        - Digital Library: UMC L130E Low Leakage FSG Library
        - Memory: 55+8 kB
        - Peripherals: 6
        - Interrupts: > 30 are available
        - Clock: Between 8 MHz (or lower) to 16 MHZ
        - Supply voltage: 1.0-1.2 V
        - Extras: debug port; reset;
        - List of Peripherals, Peripherals reflect the access block registers:
            - AFE + Sensor Biasing
            - Analog Input Matrix
            - DC-DC Power Supply
            - Multiplier by HW
            - SPI (one per channel)
            - UART

- **Accelerators**
  - Objectives: implement more efficiently (in terms of power consumption) a set of common algorithms:
    - FIR / Polynomial calculations
      - Core:
      - Digital Library: UMC L130E High Speed FSG Library
      - Clock: 8-16 MHZ
      - Supply voltage: 1.1-1.2 V

Analog Front-End

Objectives:

- Sensor selection analog bidirectional switching matrix with a number of 58 sensor pads.
- Include two analog channel processing paths.
- Maximize the programmability of the AFE
- Building blocks operating at 0.9 V, in order to reduce power consumption. However, this level of supply voltage can restrict the input dynamic range, impacting the measurement accuracy and linearity of high level resistive sensors.

Input Sample/Hold with programmable gain

- Input impedance: 50 kΩ with additional pads provisioned in case an external buffer would need to be added to provide higher level input impedance.
- Gain up to 35 dB. Additional gain obtained by cascading two of them.
- Linearity and SNDR, compatible with the 10-12 bit system
- Flicker noise reduction with chopping
- Clock: 1 MHz
- VDD: 0.9 V

Programmable Bandpass filter

- Input impedance: 50 kΩ with additional pads provisioned in case an external buffer would need to be added to provide higher level input impedance.
- Frequency range: 1 to 10 kHz
- Clock: 1 MHz
- VDD: 0.9V

High Impedance input buffer with notch (low frequency) filter

- To eliminate the 50 Hz and other low-frequency tone
- VDD: 0.9V

SDM ADC

- Input impedance: 900 kΩ.
- Resolution: 10-12 bits; with decimation and filtering can reach up to 14 bits
- Input range: 0.9 V, differential
- Two modes: 10k and 20 kHz input bandwidth
- Clock: 8 MHz
- VDD: 0.9 V
- Include low pass digital filter plus the decimator, operating at 1.2 V

Low frequency quadrature oscillator

- For the excitation of the conductivity sensor
- Frequency range: 1 kHz up to 20 kHz
- VDD: 0.9 V

Input selection matrix

- Bidirectional switches with a maximum of 200 Ω for the on resistance

- Up to 3-4 switches in series is considered
- Volatile memory for saving the matrix configuration. After power off, the matrich need to be reprogramed.

Sensor biasing

Table 7 – Sensor Biasing

		BIASING VALUES						
SENSOR	Frequency Measurements (Hz)	Duty Cycle (%)	DAC Range	DAC Current (uA)	DAC Current Max (uA)	DAC Voltage (mV)	DAC Voltage Max (mV)	Type
NANO TUBE	0.1	10	0-32uA	5	10	NA	NA	DC measurement
TEMPERATURE	0.1	10	0-2mA	1000	1000	NA	NA	DC measurement
CONDUCTIVITY	0.25	50	NA	1	10	NA	NA	AC signal at 5kHz
PRESSURE	0.1	10				NA	NA	DC measurement
FLOW								DC measurement

Power and Energy considerations

Objectives:

- DC-DC converter 0.9V and 1.2 V for supplying internal circuits
- Externally it should be “driven” by a supercap
- Capable of delivering 16 mW.
- External Rectifier for the AC power harvester

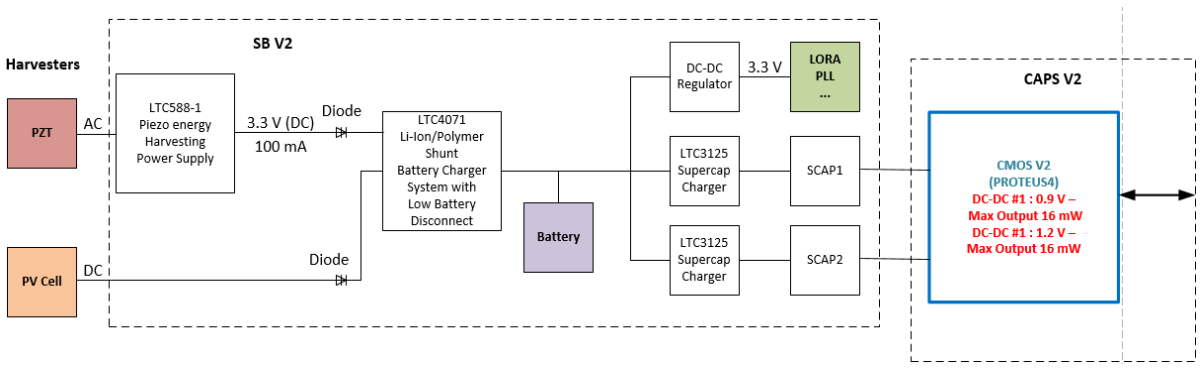


Figure 9 : Power and energy Scenario for PROTEUS4.

- The CMOS chip will be powered by two supercapacitors that can be charged up to 2.3V and 2.7 V. Internally the CMOS chip Version 2 (PROTEUS4) includes two power DC-DC converter with outputs of 0.9V and 1.2V respectively. Each DC-DC can deliver an output power up to 16 mw. Therefore the total available power is 32 mW.
- Each DC-DC power converter can indicate an estimation of the supercap charge state and an estimation interval of the power that is been used. Each one have a 3 bit word that is processed by the oMSP430.
- It is assumed that the interface with the two of types of harversters and the battery is implemented outside the CMOS chip, in the SB V2 (not in the CAPS part)

4.3.2 Analog design

4.3.2.1 Previous blocks designed in Version 1

As described in D2.1 and D3.3, several blocks of the analog front-end (AFE) have been designed, implemented and tested, namely:

- Sigma-Delta Modulator for the ADC
- Sample-hold with programmable gain
- Programmable Filter
- Input analog Matrix
- DC-DC converter.

All of these blocks will be used in version 2 and 3.

4.3.2.2 High impedance input buffer with embedded 50-60Hz notch filter

The high impedance input buffer with embedded 50-60Hz notch filter uses a discrete-time (Z-Domain[2]) signal processing approach. It is built from a switched-capacitor (SC) network with low gain amplifiers, in order to avoid power hungry high gain amplifiers. The notch filtering is obtained by combining a bandpass section, shown in Figure 30, with an adder SC branch with one possible implementation show in Figure 11.

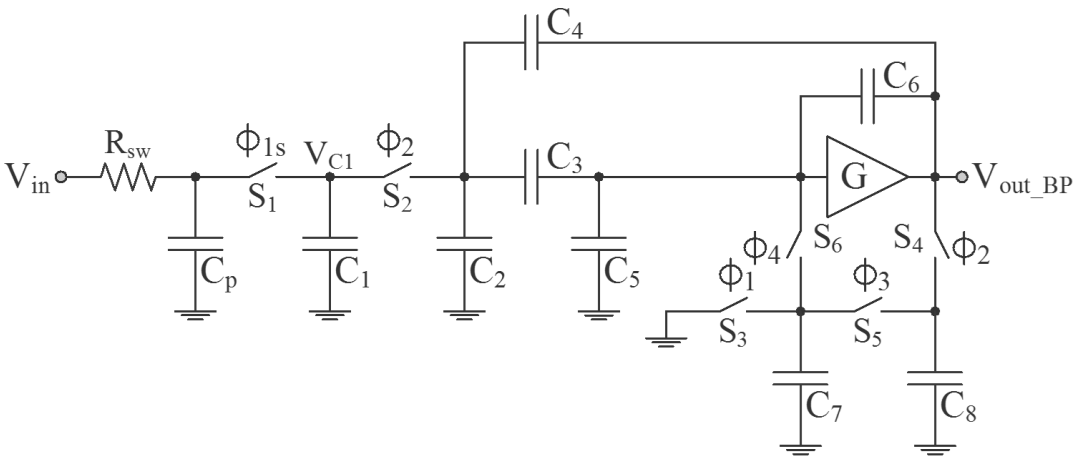


Figure 10 : Bandpass section of the high impedance input buffer.

Regarding the bandpass section, due to the high clock frequency (F_s = 2 MHz) in relation to centre frequency (f_c = 50 Hz), capacitors C_1 and C_7 are very small (1~5 fF) when compared to the remaining ones (1~10 pF). To increase the value of C_1, resistor R_{sw} (in the MΩ range) is used to increase the time constant in node V_{C1}, forcing incomplete settling in this node. Using a very large resistor and a higher valued C_1 (≈ 1pF), only a small amount of charge will be stored in C_1, effectively having the same behaviour as using a small capacitor with complete settling.

[2] Alan V. Oppenheim, Alan S. Willsky, and S. Hamid Nawab. 1996. Signals &Amp; Systems (2nd Ed.). Prentice-Hall, Inc., Upper Saddle River, NJ, USA

To increase the value of C_7, two switches (S_4 and S_5) and capacitor C_8 (which has the same value as C_7) are used. Using this configuration the value of C_7 (and C_8) can be increased. The closer the gain of the amplifier is to 2 the higher will be the increase in capacitor C_7 (and C_8), i.e, the amount of charge C_7 steals from the input node of the amplifier during phase φ_4 needs to be very small (small C_7), with G ≈ 2, capacitor C_8 is used to pre-charge C_7 with approximately the amount of charge it is supposed to have when phase 4 is turned on, so a higher valued C_7 can be used. In term of clock phase used, Phase φ14 is high when φ1 and φ4 are high. Phase φ23 is high when φ2 and φ3 are high.

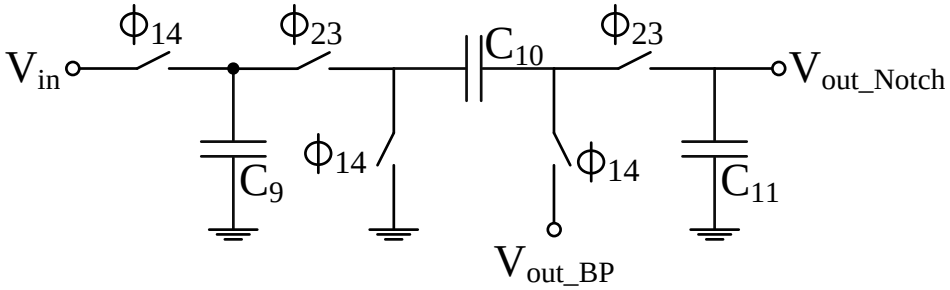


Figure 11 : SC adder branch for the high impedance input buffer.

As stated previously, to obtain a band-reject filter behaviour using a bandpass filter, an adder is used to subtract the output of the bandpass filter (f_c = 50 Hz) to the input signal, removing the 50 Hz component from the input signal (V_{in}). To perform the subtraction operation using the adder, the input signal (V_{in}) and the output of the bandpass filter (V_{out_BP}) must be in phase opposition.

The frequency response of the high impedance input buffer was obtained from electrical simulations using a 130 nm CMOS technology, which is depicted. It clearly shows the high degree of rejection of in the 50 Hz range.

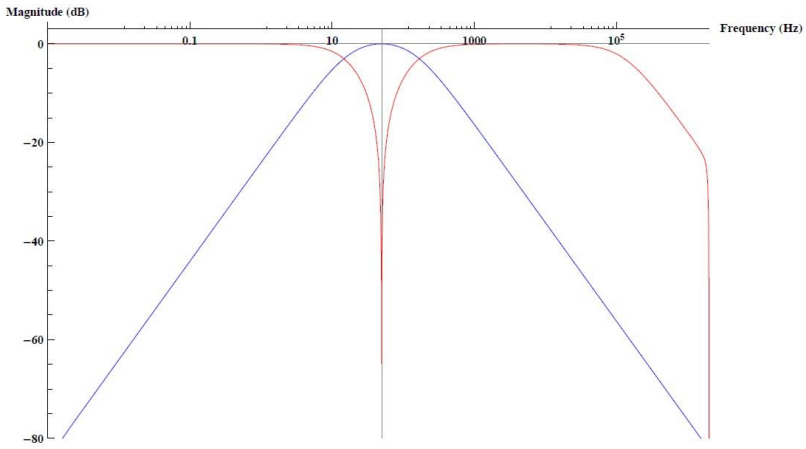


Figure 12 : Frequency response of the high impedance input buffer: (blue) bandpass (red) notch .

4.3.2.3 Low Amplitude, Low Frequency Oscillator for the Conductivity Sensor

Figure 13 shows the simplified block diagram of the analog front-end interface for the water conductivity sensor. An input current AC source is connected to the outer electrodes while the inner electrodes are used for signal voltage sensing. This signal directly reflects the level of the water conductivity since the impedance between the electrodes is strongly determined by this parameter.

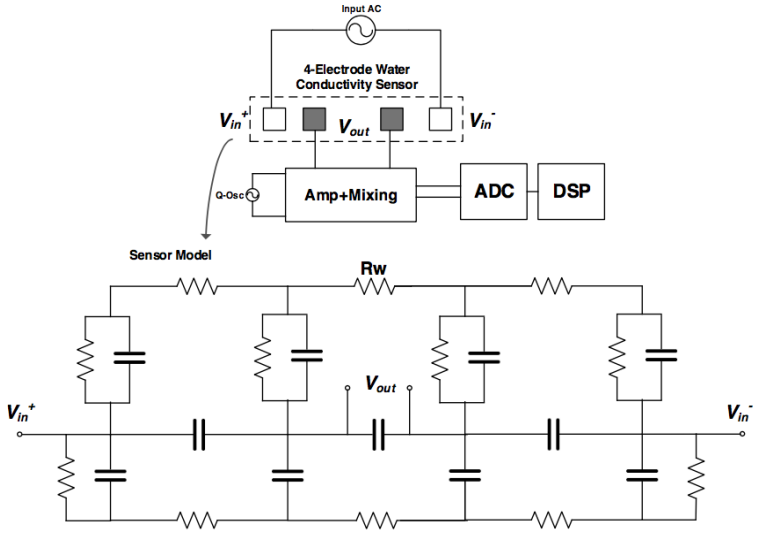


Figure 13 : Electrical model of the Conductivity sensor and its insertion in the acquisition signal path.

Considering the electrical model of the 4-eletrode sensor shown in Figure 13, the water conductivity is represented by the resistor Rw. However, the complete cell model includes several parasitic effects, including resistive and coupling capacitances, which originates a complex frequency response that narrows the bandwidth in which the conductivity can be easily determined. Usually this range locates at a few kHz. Sweeping the input signal frequency, by means of a programmable low frequency oscillator, the conductivity measurement can be obtained by using an measuring the output differential voltage.

The oscillator circuit represented in Figure 14 , has two-integrators in a feedback structure. The two integrator oscillator is a quasi-linear RC oscillator, where it is possible to have a low oscillation frequency and wide tuning range (more than one decade). Each integrator is realized by a differential pair (transistors M) and a capacitor (C). The oscillator frequency is controlled by Itune. There is an additional differential pair (transistors ML), with the output cross-coupled to the inputs, which performs two related functions:

- compensation of the losses due to R to make the oscillation possible (a negative resistance is created in parallel with C);
- amplitude stabilization, due to the non-linearity (the current source Ilevel controls the amplitude);

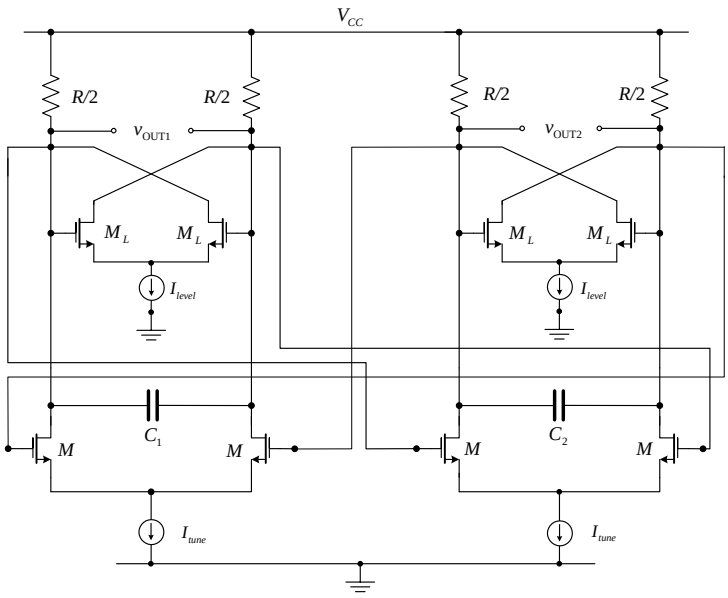


Figure 14 : Two RC-integrator oscillator in a cross coupled configuration.

The circuit in Figure 14 can be represented by the linear model in Figure 15, where the negative resistance is realized by the cross-coupled differential pair (ML), and R represents the integrator losses due to the pairs of resistances R / 2.

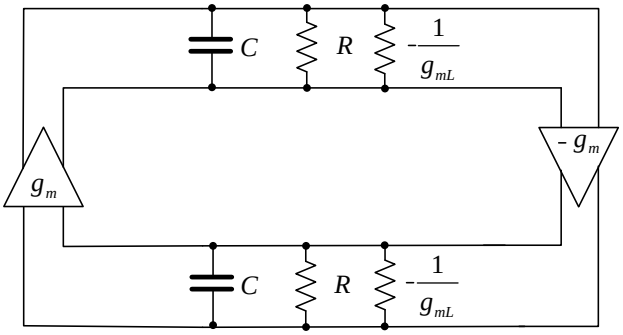


Figure 15 : Two RC-integrator oscillator small signal, linear model.

From the model in Figure 15 which is valid for quasi-linear performance, we can obtain the oscillator frequency considering that the losses must be compensated ($R_p = 1/g_{mL}$). In this case, using the Barkhausen criterion the oscillation frequency is given by:

$$\omega_0 = \frac{g_m}{C} \qquad (1)$$

From the previous equation, we can conclude that the oscillator frequency varies by changing either the capacitance or the transconductance. In a practical low frequency circuit we can change a tuning current and therefore the transconductance. Since we can change the transconductance in a wide range, these oscillations have wide tuning range as required in our impedance measurement for IoT applications.

The quadrature outputs of the oscillator can reach a value as low as 100 µV of amplitude leading to only 10 nA current to the electrodes, as shown in Figure 16. Moreover, since an output driver/buffer is added to the oscillator output, the amplitude can be further adjusted to the sensor in order to maximize its lifetime.

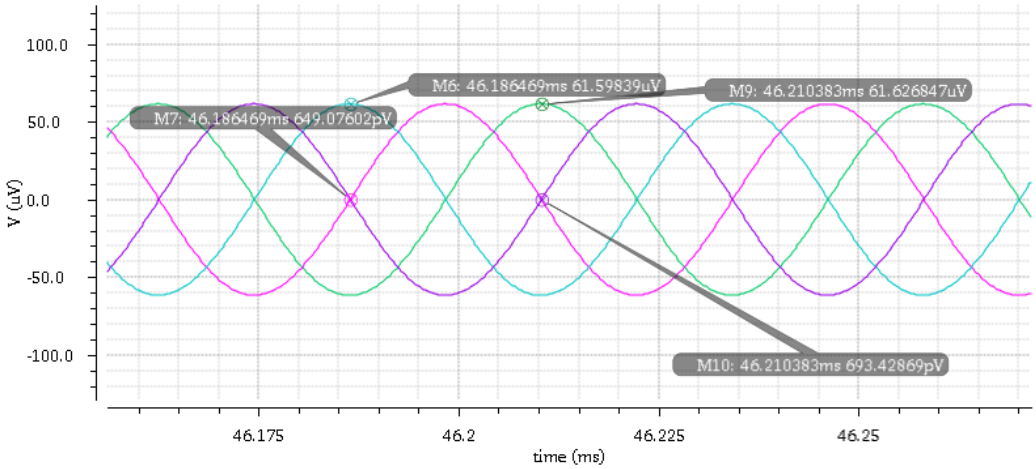


Figure 16 : Electrical simulation of the Two-RC Integrator with quadrature outputsl.

4.3.2.4 Improved DC-DC for the Power Managament Unit

A SC DC-DC converter, such as the 2:1 step down converter shown in Figure 17, works by transferring charge from the input voltage (V_{in}) to the output load (R_{out}) through the flying capacitor (C_u). The average current value in Rout is equal to the amount of charge transferred divided by the clock period. For a given output power level (P_{out}) in order to have a given output voltage (V_{out}), the clock frequency (F_{clk}) is given by expression (2), where α is the percentage value of the top parasitic capacitance when compared to C_u. This equation shows that F_{clk} is proportional to Pout (assuming constant Vout).

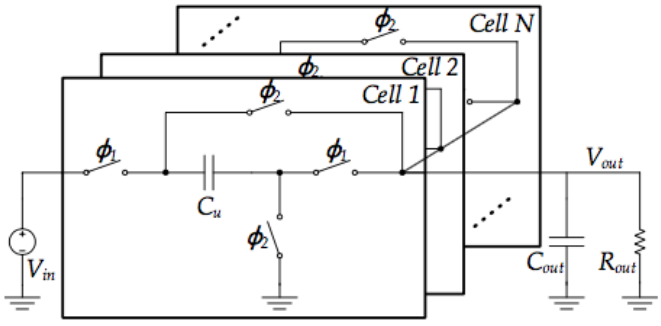


Figure 17 : Simplified schematic of the Multi cell 2:1 step down SC DC-DC converter.

An asynchronous state machine (ASM) can be used to create the clock signals with a Fclk value that guaranties that Vout is constant independently of Pout. In this case, capacitor Cu is sized to guaranty that the maximum Pout can be achieved with the maximum Fclk of the circuit. When Pout is much smaller than the maximum Pout value, Fclk becomes very small, resulting in a long time between charge transfers from Vin to Vout. Since Cout can not be arbitrarily large, this can translates into a large ripple in Vout (Vripple). Vripple is proportional to Iout and inversely proportional to Fclk and Cout.

$$F_{clk} = -\frac{P_{out}}{C_u V_{out}\left(V_{out}(4+\alpha) - V_{in}(2+\alpha)\right)}$$
$$V_{ripple} \propto \frac{I_{out}}{F_{clk} C_{out}} \qquad (2)$$

There are two conflicting requirements to size C_u: C_u should be large to obtain a high Pout and should be small to minimize Vripple when the required Pout is smaller. It is possible to overcome this by changing the value of C_u according to the value of Pout: when Pout is small a small Cu is used, when Pout increases, C_u is increased by adding more capacitors in parallel to Cu. Hence, instead of having a single SC converter with a large Cu (single-cell converter) it is possible to use several SC converters with a smaller C_u in parallel (multi-cell converter). In order to further reduce Vripple when Pout is small, the Cu capacitors of the disabled cells are connected to V_{out} resulting in an increase of the total output capacitance. This increase in C_{out} combined with the reduction of charge per clock pulse, greatly reduces the output voltage ripple. The design of each cell C_u is carried out using (3). First,

the minimum power (P_{out_min}), maximum frequency (F_{max}), maximum time between each φ1 pulse (Tm), minimum input (Vinmin) and V_{out} needs to be fixed. The minimum frequency (F_{min}) is set by $F_{max}/(1+T_m F_{max})$. Then, the C_u value of the first cell is set by the minimum required power at the maximum frequency (3). The C_u of each next cell is designed in order to keep the F_{clk} between F_{max} and F_{min}.

$$C_{cell_n} = \begin{cases} -\dfrac{P_{out_{min}}}{F_{max} V_{out}\left(V_{out}(4+\alpha) - V_{in_{min}}(2+\alpha)\right)}, & \text{for } n=1 \\ C_{cell_1}\left(\dfrac{F_{max}}{F_{min}}\right)^{n-1} - \sum_{i=1}^{n-1} C_{cell_i}, & \text{for } n>1 \end{cases} \qquad (4)$$

Capacitor C_u is implemented with a PMOS capacitor, with a top and bottom parasitic capacitance of α ≈ 7.5 % and β ≈ 0 %, respectively; a P_{outmin} of 1 mW, a number of cells of 5, a F_{max} of 10MHz, a T_m of 50 ns, a V_{inmin} of 1.1(minus a margin of 0.05 V), and a V_{out} of 0.5 V were chosen. This value of Vout was chosen so that the efficiency is maximum when V_{in} = 1.2 V. The value of each cell Cu, computed using (3), and the ON resistance of the switches (R_{on}) values at 4τ. At the maximum power, the sum of each C_u cell is equal to the C_u of the single-cell converter. And also, the parallel of each cell R_{on} is equal to the R_{on} of the single-cell converter. Hence, at full power the multi-cell converter behaves exactly as a single-cell converter. However, reducing the power will reduce the number of active cells, and thus decreasing the total value of C_u.

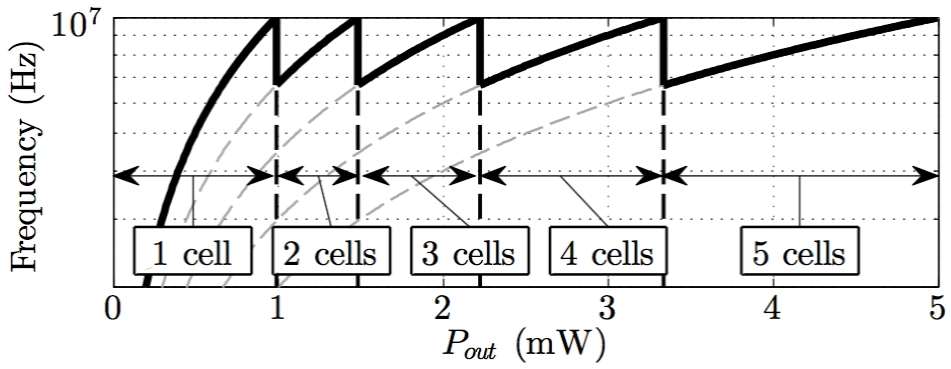


Figure 18 : Operation frequency range of the 1:2 SC DC-DC multi-cell converter for Vin = 1.05 V, Vout = 0.5 V, Cout = 71 nF.

Figure 18 shows F_{clk} as a function of P_{out} (1) for V_{in} = 1.05 V, and V_{out} = 0.5 V. The bold line show the values of frequency as P_{out} increases. each cell is activated when F_{clk} reaches the maximum frequency.

When the next cell is activated, F_{clk} changes to the minimum frequency. The cell controller requires that the frequency range is kept within these limits to work properly.

Using this evolved technique, the DC-DC of the first version, described in D2.1 and D3.3, can be further improved to reach a high output power capability, while optimizing chip area and reach an output power up to 16 mW.

4.3.3 Digital design

4.3.3.1 Microcontroller unit

The architecture of the microcontroller to be integrated in PROTEUS CMOS chip is based on a synthesizable 16-bit core. This is a Von Neumann architecture with a single address space for programming and data storage. It is compatible with the Texas Instruments MSP430 microcontrollers. The choice of this model is justified when low power 16-bit computation is required, and also by the availability of multiple resources as code compilers and debuggers, linkers. The core has a full instruction set support while also addressing modes, maskable and non maskable interruption and low power modes are supported. The memory size can be configured both for program and data memory and it also counts with a serial debug interface.

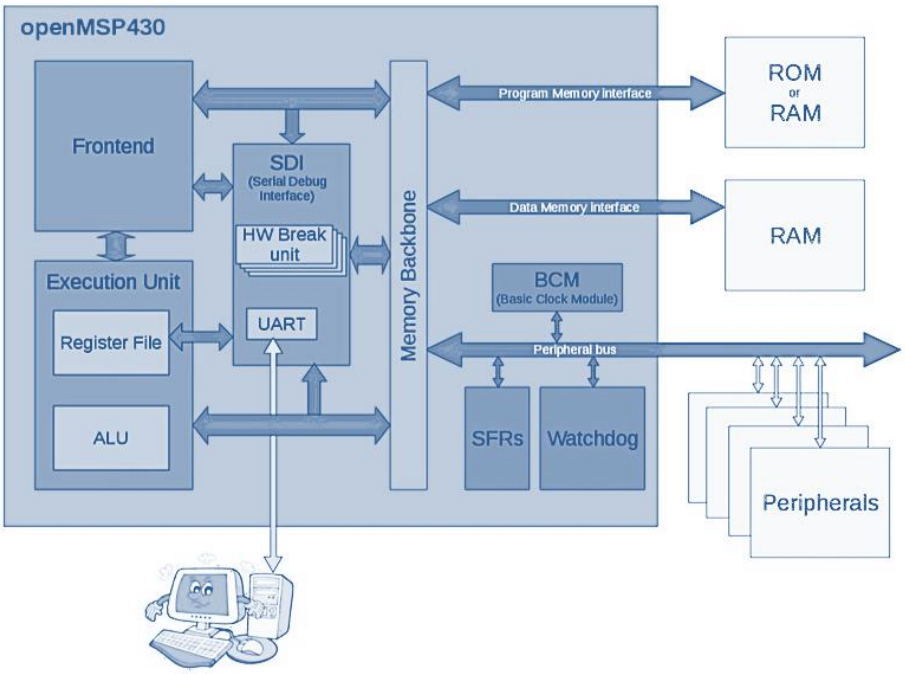


Figure 19 : openMSP430[3] block diagram.

The core schematic diagram is depicted in Figure 19 showing its principals blocks. The OpenMSP430[3] core is organized of six modules:

• Front-end: This module performs fetch and decode tasks.

[3] O. Girard. (2010). [Online]. Available: http://opencores.org/ocsvn/openmsp430/openmsp430/trunk/openmsp430

• Execution Unit: This module contains the ALU and the register file, it also executes the current instruction.

• Serial Debug Interface: This is the debugging unit, communication with the host is done with a serial interface. Four hardware breakpoint units have been included. It can run, stop or reset the CPU and also read and write on the fly the memory and the CPU registers.

• Memory Backbone: This block performs a simple arbitration between the frontend and execution-unit for program, data and peripheral memory access.

• Basic Clock Module: Generates the clock enable signals.

• SFRs: The Special Function Registers block contains diverse configuration registers (NMI, Watchdog).

• Watchdog: This is the watchdog block of the system to recover from undesired lost state.

• Multiplier: A hardware 16x16 multiplier is included.

In regard to the interrupts service, the priorities are compatible with the original MSP430, giving the highest priority to the reset, followed by the non maskable interrupt (NMI), and then with the fourteen configurable IRQ's. When two interrupts are pending simultaneously, the higher priority interrupt will be serviced first.

The main core is surrounded by some peripherals and includes program memory and data RAM memory. The openMSP430 will be synthesized in the CMOS 103 nm technology node, using standard cell digital library provided by the foundry. In order to reduce power in sleep mode, a low leakage option is chosen.

The number of peripherals will reflect the structure of the overall microsystem:

- The Analog Front End peripheral
- Multiplier peripheral
- 2 SPI +1 Serial peripheral
- PMU peripheral

4.3.3.2 Memory

The maximum memory size supported by the microcontroller is 64 kB, which should be distributed between program memory and data memory. This memory will be of type SRAM, which is a volatile. To store data and program code, a non-volatile memory of type Flash will be added to the PNODE outside the CMOS chip. A SPI connection will support the communication between the openMSP430 core and the Flash memory.

With respect to the SRAM which will integrated in the chip, is generated from the standard library supplied by the manufacturer. The FSC0L_D_SH is a synchronous high density, Low Leakage single port SRAM. It is implemented according to UMC's 0.13um 1P8M 1.2V Low Leakage CMOS process design rules and can be incorporated with Faraday's 0.13um standard cells. Different combinations of words, bits, and aspect ratios can be used for generating the most desirable configurations.

Features:

- Synchronous read and write operations
- Full custom layout density per customer configuration
- High density, available for 1.08V ~ 1.32V
- Automatic power down to eliminate DC current
- Clocked address inputs and CS to RAM with CK rising edge
- Clocked WEB input pin to RAM with CK rising edge
- Clocked DI input pins to RAM with CK rising edge

- Byte write or word write operations available
- Verilog / VHDL timing / simulation model generator
- SPICE netlist generator
- GDSII layout generator
- Memory compiler preview UI (memaker)
- BIST circuitry supported

Multi-block options for the best aspect ratio

5 Multiparameter Sensor Chip

5.1 Enhanced fabrication process flow for full co-integration (including pressure sensor)

Version V2 of the MEMS platform is intended to co-integrate on a single monolithic silicon chip, all the physical and chemical sensors targeted in the frame of the PROTEUS project. Especially the additional integration of a pressure sensor based on a single-crystalline membrane and polysilicon piezoresistive strain gauges significantly increased the number of steps of the fabrication process flow in comparison with the former version V1 based on glass substrates.

The side view of the new generation of multi-sensor chip is schematically presented in Figure 20. It gives an overview of the different technological layers used to produce the PROTEUS V2 chips. One can notice that the backside of the silicon wafer is partially etched in order to create the membrane for the pressure sensor together with a second membrane intended to sustain the resistors of the flowrate sensor so as to insure a better thermal insulation.

A second wafer made of borosilicate glass is bonded to the silicon wafer in order to create a cavity under vacuum on the backside of the membrane of the pressure sensor thus making possible to obtain an absolute pressure sensor.

All the fabrication steps of the MEMS chip platform are performed in a cleanroom environment at ESIEE, leading to full co-integration of all 4 types of physical sensors as well as arrayed slots of metallic electrodes pairs, intended to further co-integration of 5 different types of chemical sensors. Then, further CNT processing of this chip by IFSTTAR is the final step of the multi-sensor integration on this V2 MEMS chip multi-sensor platform.

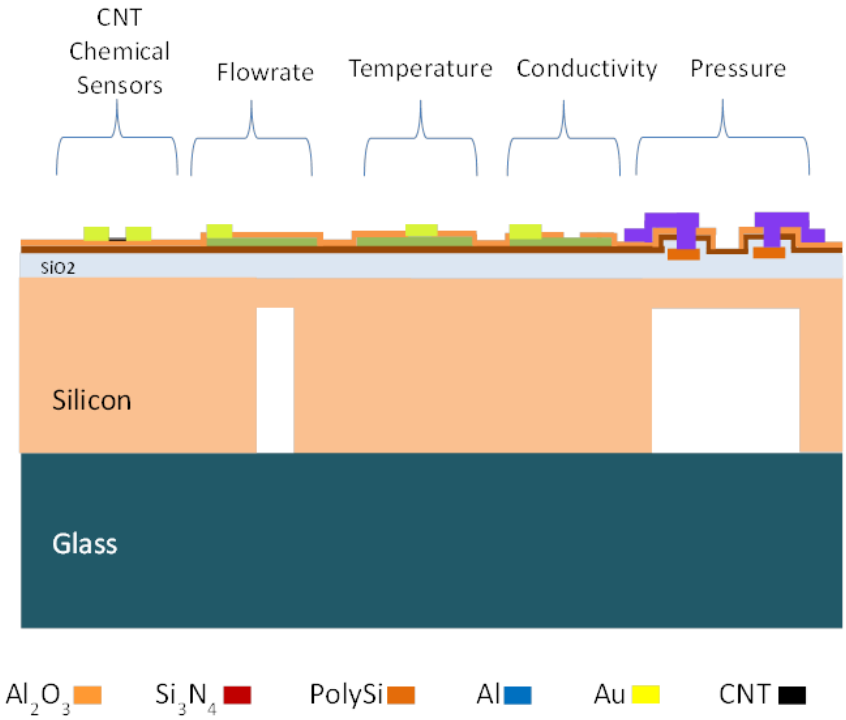


Figure 20: Side-view of the sensor chip

To successfully implement up to 7 physical sensors and 9 chemical sensors (including redundancy) on a single chip, a new fabrication process flow has been elaborated based on the following strategy:

- The fabrication steps required to obtain the pressure sensor are planned first, including the piezoresistive polysilicon layer for the sensing gauges and associated insulated layers.
- Then the co-integration of the other physical sensors (temperature, flow rate and conductivity sensors) is performed leading to a total of 9 mask levels and 3 levels of metallization. This sequence takes advantage of the previous process development validated in version V1;
- Then come the back-side silicon wafer etching by Deep Reactive Ion etching (DRIE);
- Then, Silicon/Glass wafer-level bonding are also part of this enhanced process flow.
- Wafers are then diced
- The final step is performed at the chip-level; it consists of CNT post-processing in order to achieve co-integration of the chemical sensors.

It is worth mentioning that two types of metallization (Al and Au) are evaluated to electrically connect the pressure sensor. As Aluminium (Al) is a standard metallization well known to exhibits a good quality ohmic contact with P-type polysilicon layer, we also consider gold layer (Au) as an alternative because it allows keeping the same metallic layer to electrically connect all the sensors of this PROTEUS V2 chip and also to provide the required base material for chemical sensors.

Atomic Layer Deposition is also used to deposit a very thin layer (10 nm) of Al_2O_3 on the whole surface of the chip –except on the electrodes for conductivity measurement, on the bonding pads and on the electrodes of CNT-based chemical sensors). This ALD coating is in this case intended to act as a final protective coating.

More details on the implementation of this fabrication sequence is presented in report D3.4.

In order to evaluate different versions of the pressure sensor, flowrate sensor and conductivity sensor, integrate redundancy for some sensors and address variable range of measurement, 3 versions of the MEMS chip platform were designed with the following features described in Figure 21 here below.

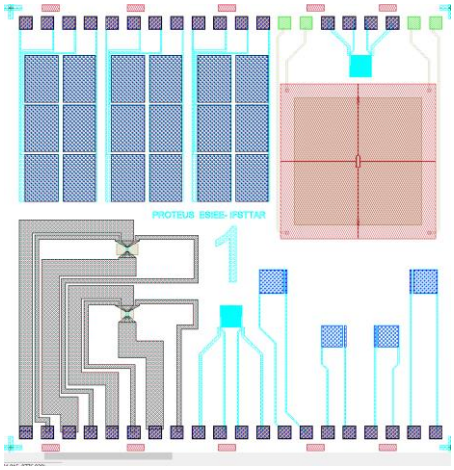
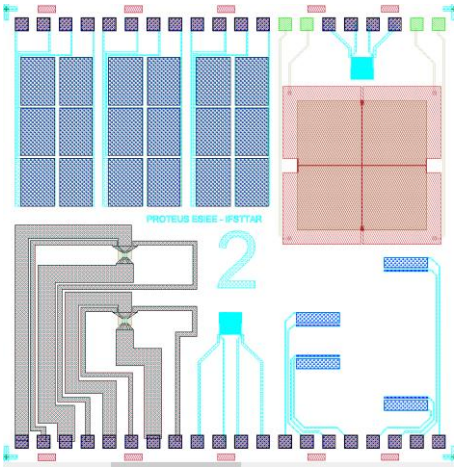
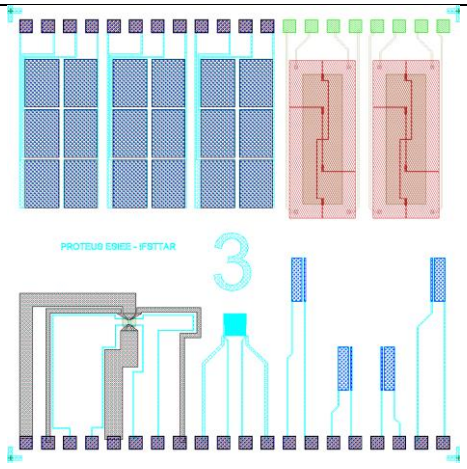
	**VERSION 1** - 2 Flow-rate sensors - 2 conductivity sensors - 2 temperature sensors - 1 pressure sensor - pH sensor - Cl_2 sensor - Cl^- sensor - NO_3^- sensor - Hardness sensor (Ca_2^+ + Mg_2^+)
	**VERSION 2** - 2 Flow-rate sensors - 2 conductivity sensors - 2 temperature sensors - 1 pressure sensor - pH sensor - Cl_2 sensor - Cl^- sensor - NO_3^- sensor - Hardness sensor (Ca_2^+ + Mg_2^+)
	**VERSION 3** - 1 Flow-rate sensor - 2 conductivity sensors - 1 temperature sensor - 2 pressure sensors - pH sensor - Cl_2 sensor - Cl^- sensor - NO_3^- sensor Hardness sensor (Ca_2^+ + Mg_2^+)

Figure 21 : PROTEUS V2 chips description.

5.2 Pressure sensor design update

The main features of the pressure sensor design have been introduced in our previous report D2.1.

This sensor is now co-integrated with all other sensors in the monolithic MEMS platform chip. This integration effort led to important updates of the fabrication process as described in the previous section.

As a reminder, the pressure sensor is based on a thin silicon thin membrane on the top of which we have four piezoresistive starin gauges (resistors) are arranged in a Wheatstone bridge configuration and made of polycrystalline silicon (polysilicon) thin film. Silicon resistors are required to take advantage of a sensitive-enough piezoresistivity (50x more than platinum resistors). More importantly, there is a need for a deformable membrane to convert the external hydrostatic pressure into mechanical stress on the resistors. These two aspects require additional materials and additional fabrication steps. These important differences in the fabrication process motivated our choice to not integrate the pressure sensor in the first version of prototype. Instead, we made its design independently but keeping all constraints of process compatibility with all other types of sensors, towards a full co-integration at the end (in the second run).

Three different designs (shown in Figure 22) were proposed for the pressure sensor and each of them have been integrated in the 3 versions of the multi-sensor MEMS platform.

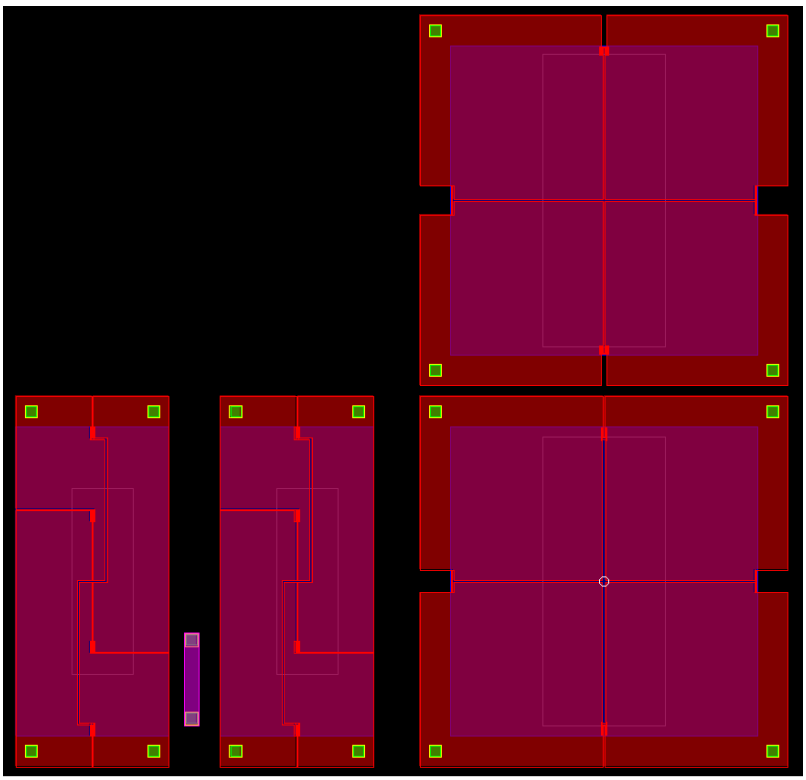


Figure 22 : Typical layouts of MEMS pressure sensors. Various versions are considered. Two versions involve a square membrane, while the last version (bottom left) considers two neighbour pressure sensors having a rectangular membrane (and a temperature sensor in-between, which provides bothtemperature compensation capabilities and redundancy – but at the expense of a reduced sensitivity, compared with the square sensors.

The behaviour of the pressure sensors was evaluated beforehand through numerical simulations based on finite element modeling (FEM). These simulations include a first set of structural simulations so as to evaluate the strain field when the membrane is deflected by a uniform pressure. Then coupled simulations, including both structural and piezoresistive led on one hand to an appropriate choice for the membrane lateral dimensions and thickness and on the other hand to optimum placing of the

resistors and appropriate choice of their dimensions. Typical results of such simulations are shown in Figure 23. They relate to the rectangular shaped pressure sensor. Those simulations show that the optimal position do not coincide with that of the maximum value of Syy; it is in this case slightly different, hence the interest of performing the above-mentionned coupled simulations.

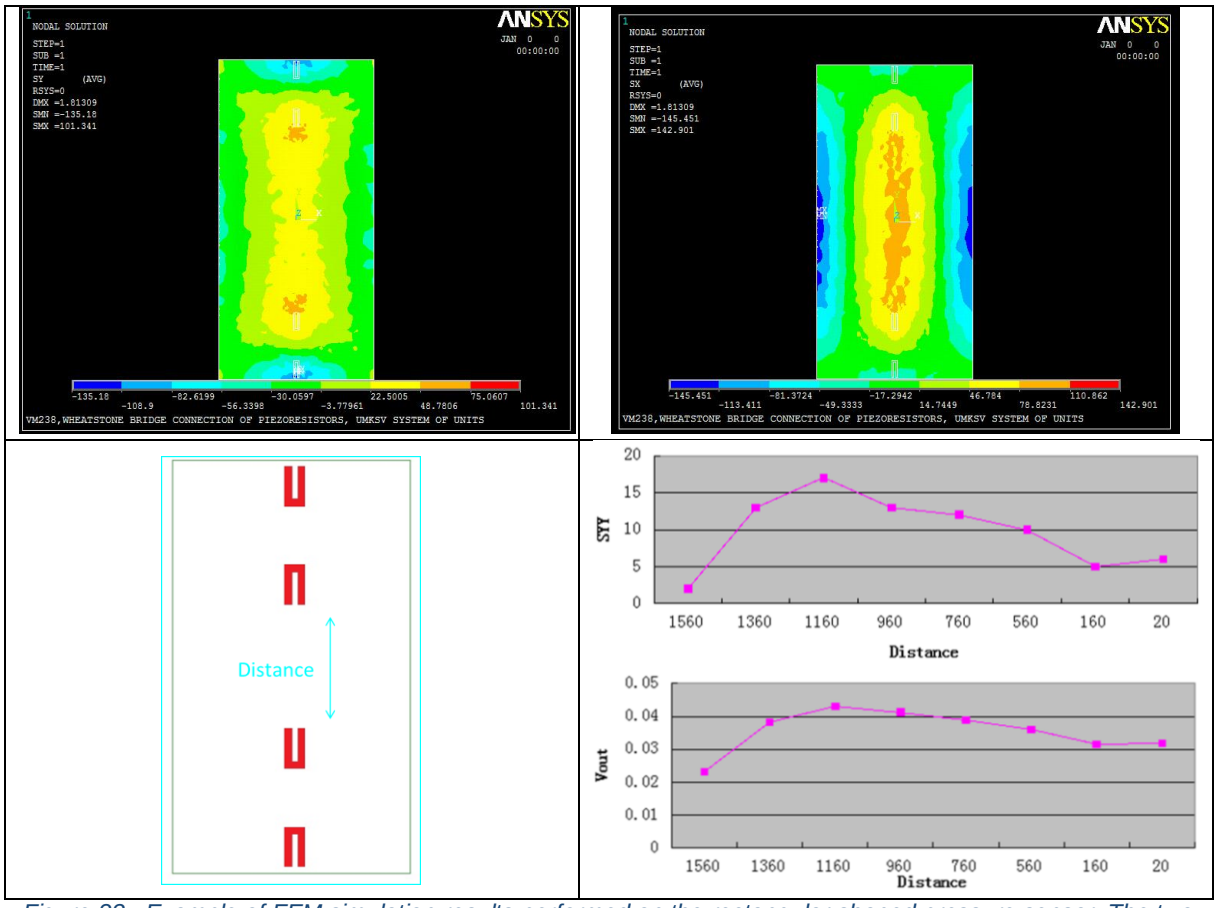
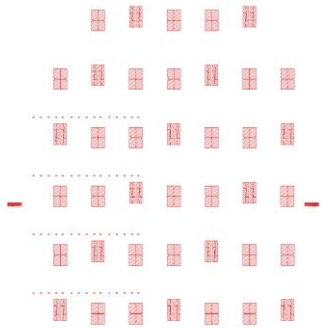
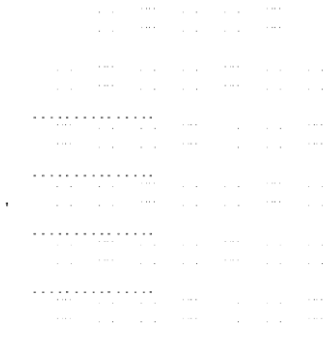


Figure 23 : Example of FEM simulation results performed on the rectangular shaped pressure sensor. The two upper contour plots show the distribution of the Sxx and Syy stress components. The lower right side curves show the effect of the position of the central resistances on the voltage at the output of the Wheastone Bridge (dimensions are expressed here in micrometers).

5.3 Mask Layout for microfabrication of the physical sensors and electrodes for further CNT processing

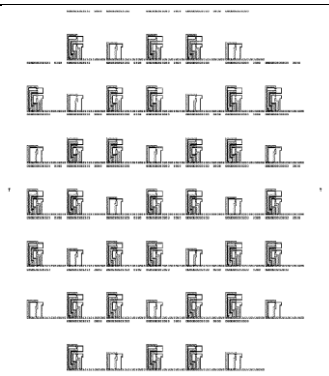


PROTEUS V2 Gauges

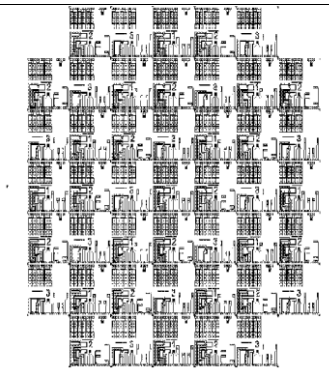


PROTEUS V2 Contacts

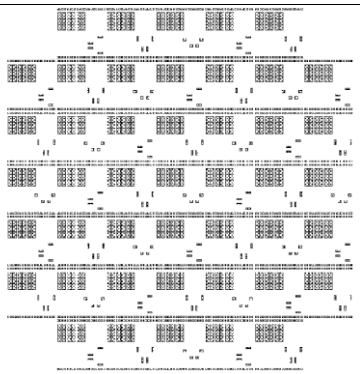
PROTEUS V2 Metal 1



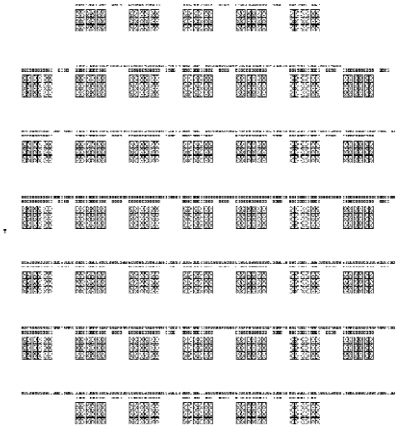
PROTEUS V2 Metal 2



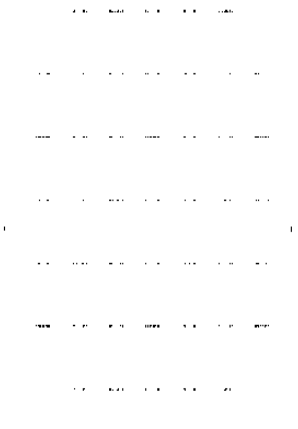
PROTEUS V2 Metal 3



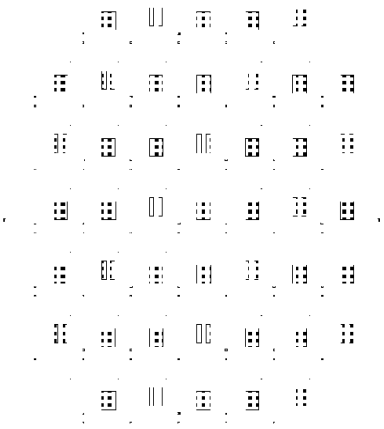
PROTEUS V2 Pads opening_All



PROTEUS V2 Pads_ Opening



PROTEUS V2 Pads_ Opening_ Pressure



PROTEUS V2 DRIE Back

5.4 Alternative designs of Flow rate sensors

5.4.1 Motivation: the absolute need for co-integration on silicon

Flow rate measurement is among the parameters of interest for water network monitoring systems. But this application also requires additional measurements such as pressure, temperature and electric conductivity, besides other chemical sensing capabilities. It is therefore tempting to co-integrate all those sensors on the same MEMS chip so as to provide a monolithic multi-parameter sensing solution and this is among the targets of the PROTEUS project. However, most of the existing flow rate sensors for air and water media are based on hot wires and fabricated on glass substrates [1,4] in order to reduce the heat leakage and minimize the hot wire consumption. But in our case the pressure sensor requires a silicon substrate. Therefore, the flow rate sensor needs to be on a silicon substrate to enable its co-integration with all other sensors on the same chip.

Motivated by the need for multi-parameter sensing chip for monitoring water networks, we address here the specific case of a flow rate sensor where the main challenge is the substrate material. Instead of using conventional low thermal conductivity materials such as glass, silicon has to be used absolutely. Indeed, a silicon substrate enables the co-integration of various kinds of sensors on the same chip as shown in the PROTEUS project. However, it will increase the flow-rate sensor power consumption due to larger thermal leaks. We therefore study an optimized low power micro-machined flowrate sensor still based on a silicon substrate and operating according to hot-wire anemometry. It can be considered as an alternative to other well established sensors for liquid flow rate measurement when both the use of a silicon substrate and low power consumption are needed.

5.4.2 Glass-substrate flow rate sensor

The flow rate sensor is composed of three platinum resistances on top of a substrate as depicted in Figure 24. The platinum resistances are 0.34-µm thick, 10-µm wide and 106-µm long. They are separated by a 20-µm wide gap. The three resistors can be used as temperature sensors while only the central one can be used as a heater through joule effect heating.

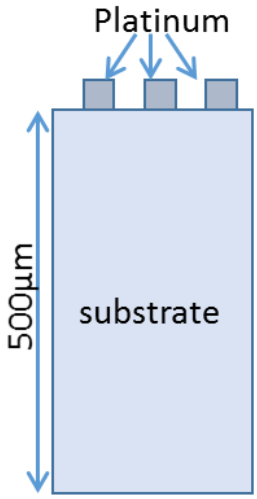


Figure 24 : standard schematic of used flowrate sensors.

The flow rate sensor can be used under both anemometric and calorimetric schemes. The anemometric scheme enables the flow rate calculation through the heater temperature decrease due to the flow cooling effect. The calorimetric scheme give access to the flow velocity through the measurement of the temperature profile, hence the temperature at different positions. Consequently, the anemometric

scheme uses the central heater only while the calorimetric scheme requires the use of the three temperature sensors.

In the present report, only the anemometric operating scheme is described. A first flowrate sensor where glass is used as the substrate material has been fabricated and tested. The sensor is supplied with a constant electric current of 10 mA. The sensor equilibrium temperature under zero flow velocity is referred to as T_{max}. Under non nil velocity flow, the sensor equilibrium temperature is smaller than T_{max}. For very large fluid velocities, the sensor temperature tends towards the fluid ambient temperature T_0.

We present in Figure 25 the sensor temperature variation as a function of the flow velocity. The non-dimensional temperature $(T - T_0)/(T_{max} - T_0)$ where T is the sensor temperature is plotted. The non-dimensional temperature ranges between 1 and 0 for nil and infinite velocity, respectively.

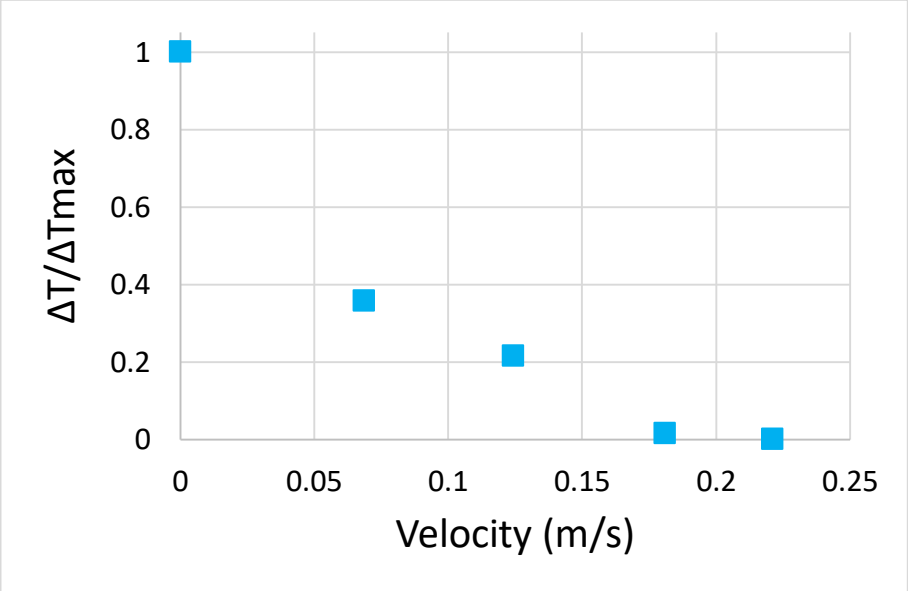


Figure 25 : non-dimensional temperature of the glass-substrate sensor as a function of the flow velocity.

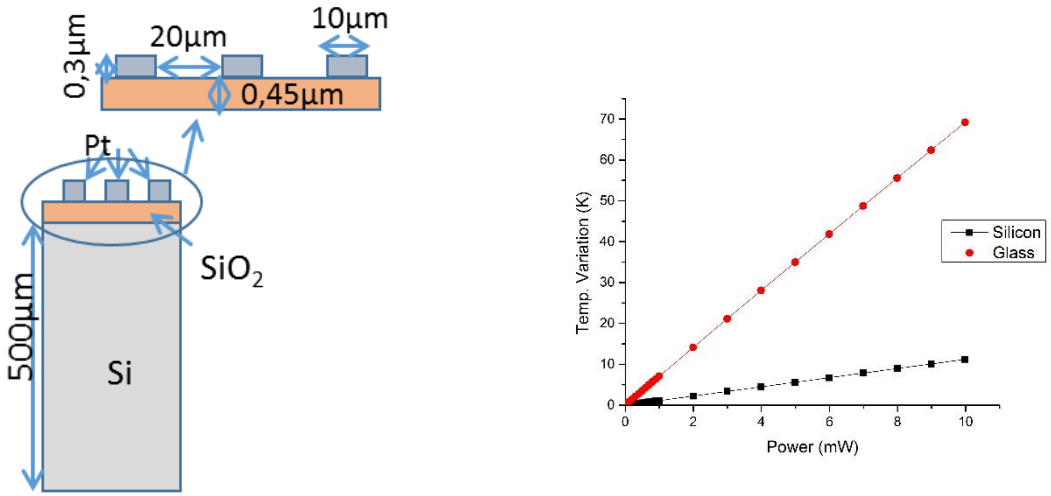
The results presented in Figure 25 show that the tested sensor is sensitive to flow velocities up to 0.18 m/s. This results means that the platinum heater is completely cooled ($T = T_0$) for velocities larger than 0.18 m/s. This limit can be easily shifted towards larger velocities if a larger electric current is used. Indeed, the larger the electric power supply, the larger T_{max} and the larger the flow velocity needed to completely cool down the heater. Consequently, a large velocity range can be covered by the present device by simply tuning the power supply.

5.4.3 The challenges of co-integration of a flow-rate sensor on a silicon substrate

In, the multi-parameter sensor, all sensors are based on resistive read-out and all of them, except the pressure sensor, are easily obtained by metal micro-patterning with the combination of Ti, Pt and gold. Hence, when using glass as a substrate material, flow-rate sensors were easily co-integrated with temperature sensors and water conductivity sensors. However, the additional co-integration with the pressure sensor required the use of a silicon substrate. In the following paragraph, we compare the silicon based flow rate sensor with the previously reported one (glass based) and highlight a few challenges.

5.4.4 Comparison between glass and silicon as substrate materials for flow-rate sensors

The second device was fabricated on a silicon substrate. A 0.45-µm thick film of SiO_2 was deposited between the silicon substrate and the platinum resistors as shown in Fig.3.a. We also show in - Fig.3.b the equilibrium temperature of the heaters under zero velocity flow for both devices, glass and silicon, respectively for different electric powers. We observe a much smaller temperature increase for silicon substrate devices for all heating powers. For instance, for 10 mW, the silicon device temperature increase is smaller than 10 °C versus more than 60°C for the glass device. According to this behaviour, we expect a lower sensitivity of the silicon device to flow velocities.



(a) (b)

Figure 26 : The flowrate sensor built on a silicon substrate (a) and the maximal temperature (under zero velocity flow) for glass and silicon devices for different heating powers (b).

The temperature variation of the silicon device versus the flow velocity is shown in Figure 27. As expected from its behaviour under zero velocity flow, the silicon sensor is much less sensitive than the glass one under the same supply power. This would induce, if comparable sensitivities are needed, a much larger power consumption. This behaviour is mainly due to the thermal properties of silicon. Indeed, silicon thermal conductivity is larger than that of glass by a factor 100. Consequently, a better thermal insulation of the heater is needed to improve the silicon sensor sensitivity without increasing the power consumption. The device thermal conductance depends on the used materials and the device geometry. Since silicon use is compulsory for co-integration needs, the control parameter for a better thermal insulation is the device geometry. In the following paragraph, we present a third device which has been investigated in order to increase the sensitivity of the silicon based device.

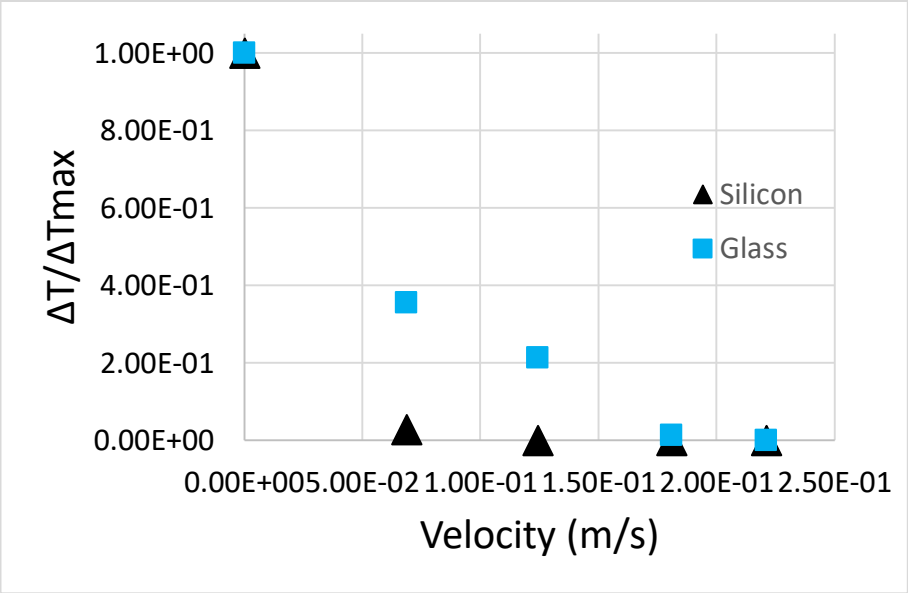
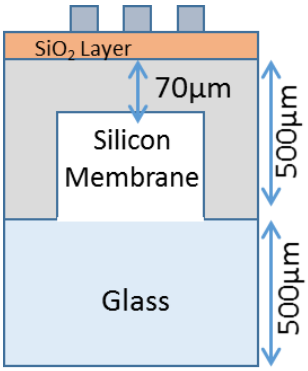


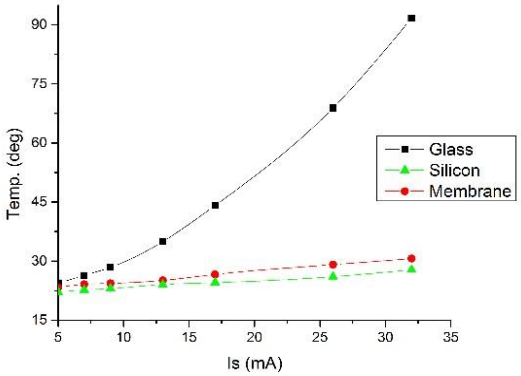
Figure 27 : non-dimensional temperature of the glass-substrate sensor and the silicon-substrate sensor as a function of the flow velocity.

5.4.5 Design and simulation of a membrane-based flow-rate sensor on silicon

In the current paragraph, we consider platinum resistors deposited on a thin glass layer on top of a silicon membrane, instead of a full silicon substrate, on top of a glass substrate as shown in Figure 28-a. The silicon membrane enables a better thermal insulation of the platinum resistors since the contact surface with the full substrate is reduced. We also show in Figure 28-b the temperature increase of the three devices under zero velocity flow for different electric currents. The membrane device temperature increase is slightly larger than that of the silicon substrate devices. Consequently, a slightly better sensitivity to flow velocity is expected for the former.



(a)



(b)

Figure 28: Flow rate sensor on a silicon membrane (a) and the maximum temperature (under no flow) for the three devices as a function of the injected electric current.

We present in Figure 29 the temperature decrease of the three studied devices as a function of the flow velocity.

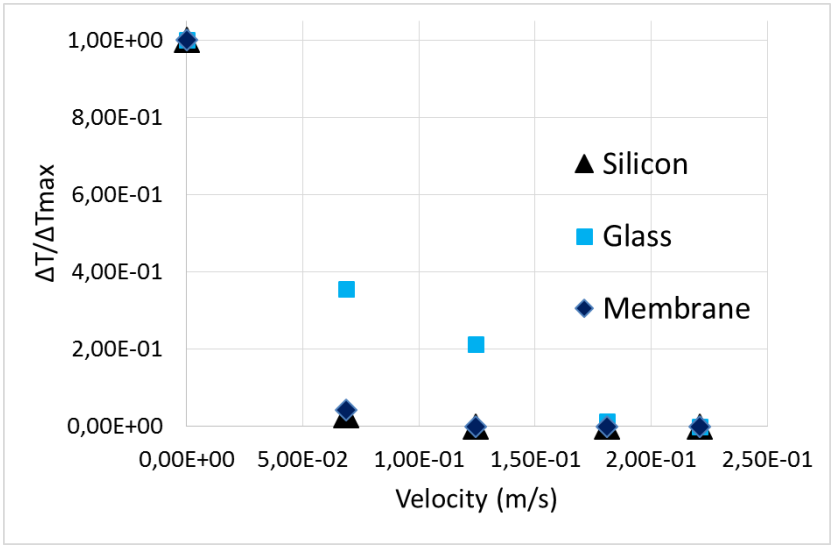
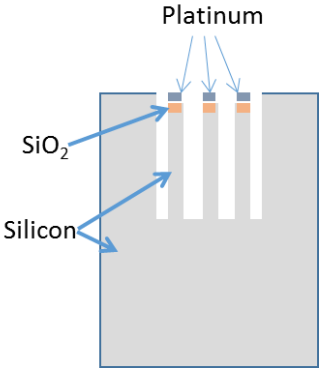


Figure 29 : non-dimensional temperature of the three devices as a function of the flow velocity.

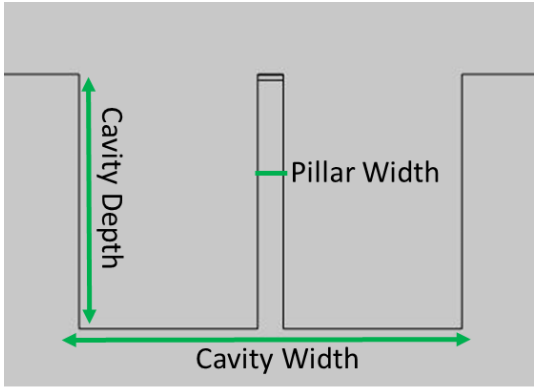
As expected, the membrane based device exhibits a slightly larger sensitivity to flowrate that the silicon substrate device. This difference can be observed for flowrates around 0.07 m/s. However, the enhancement is not significant. A better thermal insulation of the platinum heater is needed. This will be discussed in the next paragraph.

5.4.6 Design and simulation of comb-based flow-rate sensor on silicon

According to the previously presented results, the use of a silicon based substrate reduces the thermal insulation of the platinum heater and decreases the device sensitivity for a given power consumption. A geometric optimization, such as the use of a membrane, can reduce the substrate thermal conductance and enhance the device sensitivity. The results obtained with the silicon membrane as a substrate are still not satisfactory. In the present paragraph, we investigate a further optimization of the substrate geometry. The platinum resistors are deposited on a thin glass layer on top of silicon pillars in a comb like structure as shown in Figure 30-a.



(a)



(b)

Figure 30 : the comb like (a) and the single pillar (b) devices.

Since the anemometric mode is used, only the central resistor on a single pillar can be considered as shown in Figure 30-b. In addition to the resistors dimensions, the comb like or single pillar structure full specification requires two additional parameters: the pillar height and the cavity width. A full parametric study was performed on the device geometry. We show in Figure 31 the temperature decrease of the single pillar device compared to the original glass device and the corresponding silicon substrate device. The pillar is 100-µm high and the cavity is 150-µm wide.

Two versions of the single pillar device are presented here. The resistor is 0.34-µm thick and 106-µm long. In one version, it is 5-µm wide while it is 10-µm wide in the other. The glass thin layer is 0.45-µm thick. We clearly observe larger sensitivity of the pillar device with comparison to the full silicon substrate device. The performances of the pillar device are intermediate between the silicon and glass devices. They also increase when the resistor width decreases. This last trend can also be observed in glass or full silicon substrate devices even though it is not shown here.

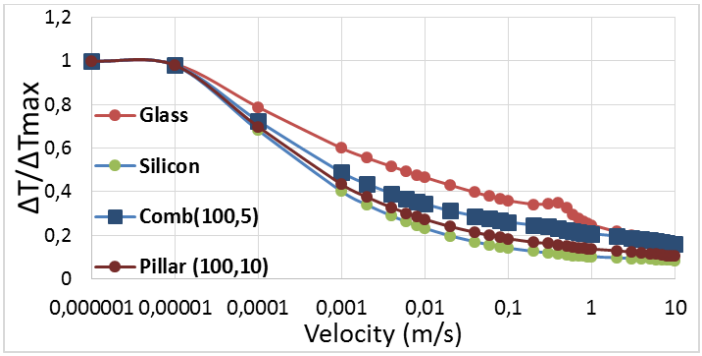


Figure 31 : Temperature decrease as a function of the flow velocity of the silicon device, the glass device and two versions of a single pillar device obtained by 2D FEM CFD simulations.

5.5 CNT sensors

5.5.1 Principle of operation

Reminder of D21: In Proteus, CNT sensors are used for chemical sensing. A random network of carbon nanotubes (CNT) is deposited between parallel metal electrodes, forming an ohmic device (Figure 32). Analytes physisorb on the CNT surface and change the overall device resistance. To ensure that the resistance change is controlled by a given target analyte, CNT are functionalized non covalently with specially designed conjugated polymers (Figure 33). Each polymer is designed to react to only a limited number of analyte in water.

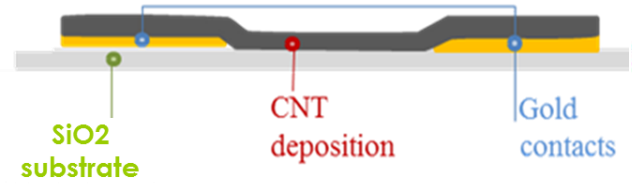


Figure 32 : Architecture of the CNT ohmic sensor

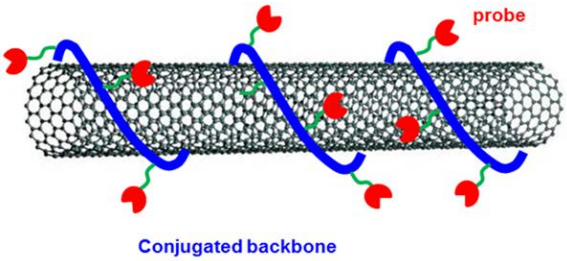


Figure 33 : principle of the non covalent functionalization for selective sensing with carbon nanotubes

5.5.2 CNT sensor versions:

The following table describes the different versions of the CNT sensors considered during Proteus project:

PNODE VERSION	Target analytes (number of devices by analyte)	CNT deposition process	Electrode features
PNODE V1, sensor chip V1.2 Evaluation in progress at caps level	pH (3), Cl- (3), Cl2 (3)	Initial process P1	Initial design D1: 3x3 sensor array Large electrodes (1,1mm)
PNODE V2, sensor chip V2.1 Evaluation at caps level mid Y3	pH (2), Cl- (2), Cl2 (2), hardness (3)	Optimized process P2	Initial design D1: 3x3 sensor array Large electrodes (1,1mm)
PNODE V3, sensor chip V2.2 Evaluated at caps level end-Y3	pH (3), Cl- (3), NO3- (3), Cl2 (3+), hardness (3+)	Optimized process P2	Optimized design D2: Small electrodes (0,6mm) 5 lines of 3 to 5 sensors

5.5.3 Optimized fabrication flow

The process used to fabricate the CNT sensors integrated into Proteus node V1/sensor chip V2.1 is described in deliverable D3.1 and deliverable D5.2. It is based on layer-by-layer inkjet printing of a different CNT ink for each type of sensors. A first layer is printed for all of the devices, for all of the inks, then the deposition on all of the sensors is dried and rinsed to remove traces of solvents, surfactant and unbound polymers. The number of layers needed to reach resistances below the 300kΩ threshold may reach up to 30.

It featured significant drawbacks:

- Limited controllability on resistance level and device positioning
- Partial mixture between the CNT inks used to realize the three different types of devices
- Leftover traces of polymer all over the chip
- Very slow process

We developed an optimized process featuring the following properties:

- Controllability of the CNT positioning resulting in increased cleanliness
- Drastic time reduction by modifying the rinsing process
- Overall improved reproducibility

The details are provided in deliverable D3.4. Figure 34 shows the outcome of this optimized process. It was observed that the relative device-to-device resistance dispersion linearly decreases with the resistance of the devices (Figure 35). As a consequence, the process should aim at the lower resistance manageable in the allotted time, if possible 100kΩ or lower (NB: in this process, the number of layers is increased until the resistance reaches the desired value)

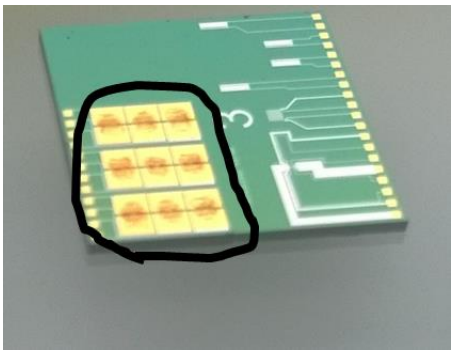


Figure 34 : Result of the optimized fabrication process

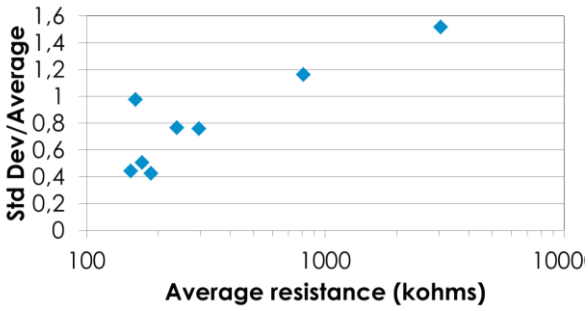


Figure 35 : Relative standard deviation over 9 devices (standard deviation over average) versus average resistance of the 9 devices. Results obtained on 8 different chips (with different number of layers)

5.5.4 Optimized electrode design

In Proteus sensor chip V1.2, integrated into Proteus V1 PNODE, the CNT sensors are fabricated on top of electrodes featuring the following design (design D1,Figure 36): length of electrode 1.1mm; spacing between electrodes 100µm; spacing between pairs of electrodes: 75µm. The devices are arranged into three lines of three, resulting in a total of 9 devices. Each set of three sensors is used to target a separate analyte, pH, Cl-, Cl2.

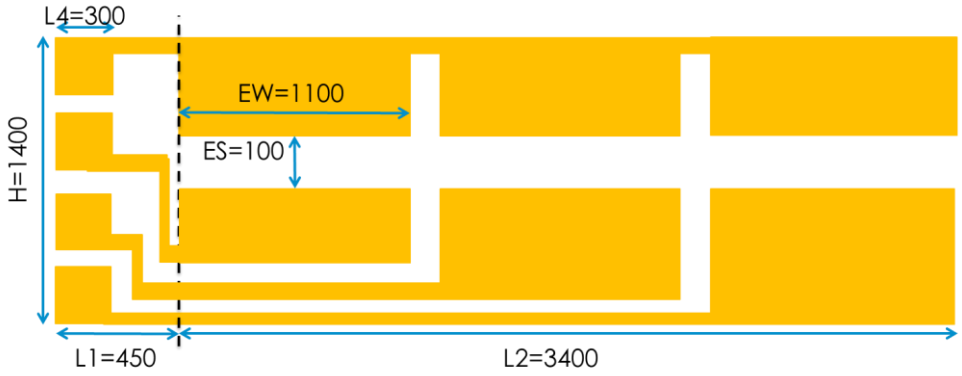


Figure 36 : CNT electrode geometry for V2.2. sensor chip

This design is used further in sensor chip V2.1. A full line of devices (3) is kept for the hardness sensors as it is the newest generation and might need more testing. There is one device of each type over the two remaining lines, pH, Cl2, Cl- (Figure 37).

One of the goals of the V2.2 sensor chip is to increase the number of multiplexed CNT devices up to at least 3x5 devices or optimally 5x5 devices. Each type of sensors will occupy a separate line, as show in Figure 38.

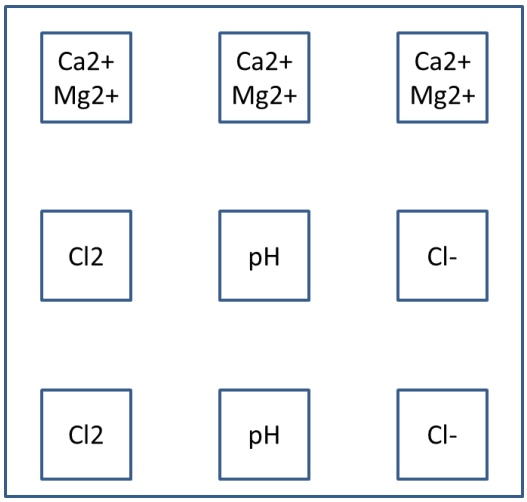


Figure 37 : Array of CNT sensors in the V2.1 sensor chip

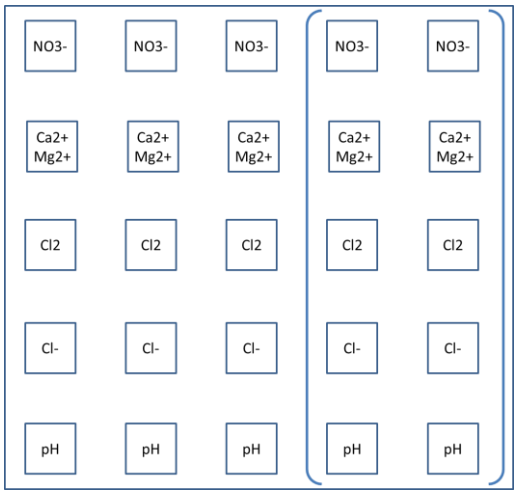


Figure 38 : Array of CNT sensors in the V2.2 sensor chip. The array is at least 3x3 and may reach up to 5 sensors for certain lines.

Increasing the number of devices while maintaining the same footprint to the whole sensor chip (11mm lateral size) requires a steep decrease in the CNT sensor footprint. To do so, the impact of electrode size and spacing on the resistances of the devices was studied. As expected the resistance decreases with increasing electrode length (quadratically) and decreasing electrode spacing (exponential) (Figure 39 & Figure 40). These quick variations in resistance are typical of percolating networks close to the

percolation threshold. Overall, the smallest CNT pattern with resistance consistently below 300kΩ featured 400µm length.

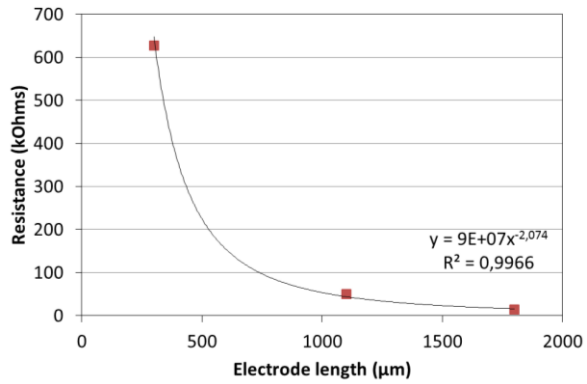


Figure 39 : Impact of the electrode length on the resistance

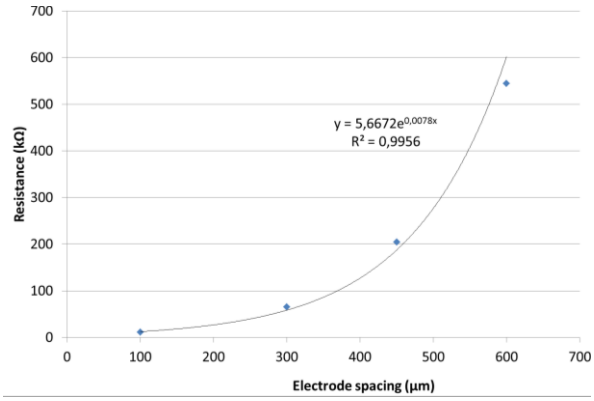


Figure 40 : Impact of the electrode spacing on the resistance.

Finally, we propose the following geometry to the V2.2 CNT electrodes (Figure 41): electrode length 600µm, electrode width 400µm, electrode spacing 100µm, device spacing 150µm. The overall footprint is reduced by 52% compared to the V2.1 version for a line of 3 devices (not counting the pads).

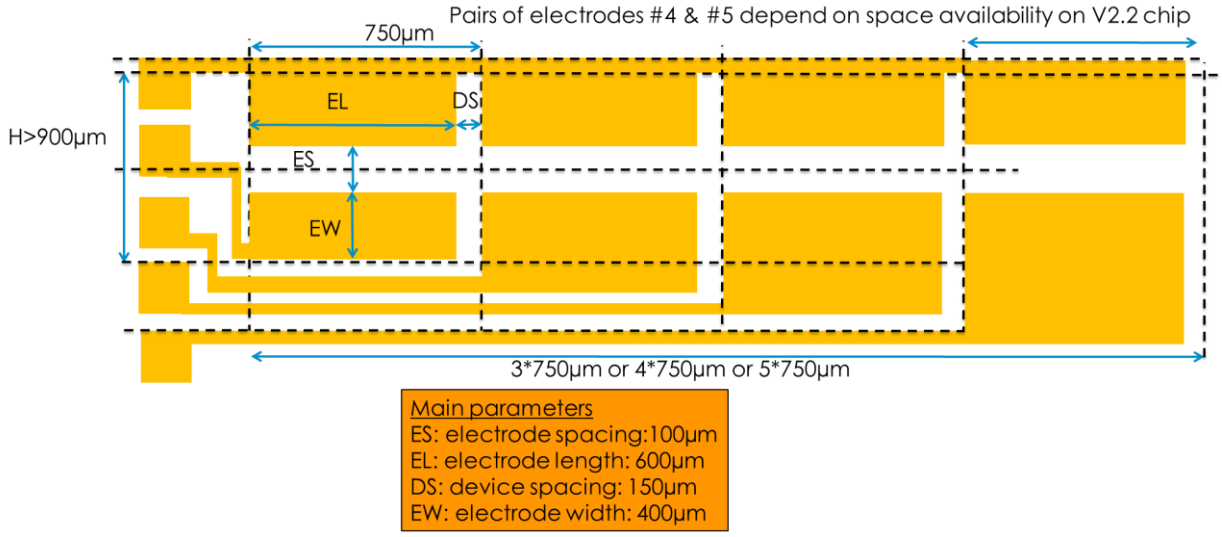


Figure 41 : CNT electrode geometry for V2.2. sensor chip.

5.5.5 Functionalization polymers

The following sections describe the novel polymers used to functionalize the CNT for selective sensing. IFSTTAR, Ecole Polytechnique & CNRS are looking for IP protection by preparing a patent to be submitted end of February 2017.

5.5.5.1 Chlorine monitoring: detection of hypochlorite

Reminder of D2.1: The detection principle is based on the recognition of hypochlorite ions ClO- using an oxime function grafted to the conjugated polymer. The selected polymer is shown in Figure 42:

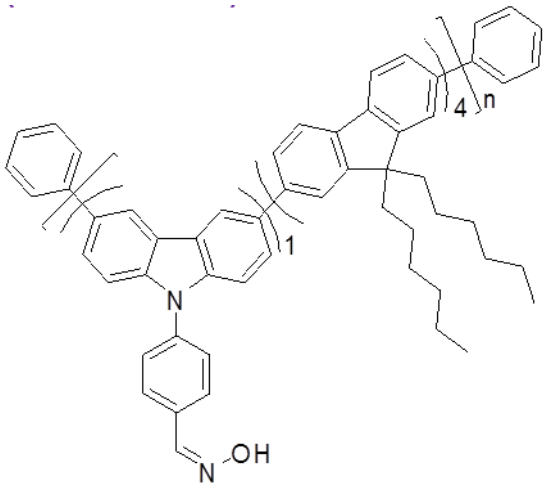


Figure 42 : Polymer for hypochlorite detection bearing oxime groups

5.5.5.2 Chloride detection

Reminder of D2.1: The detection principle is based on the recognition of chloride ions Cl- using a urea function grafted to the conjugated polymer. The selected polymer is shown in Figure 43:

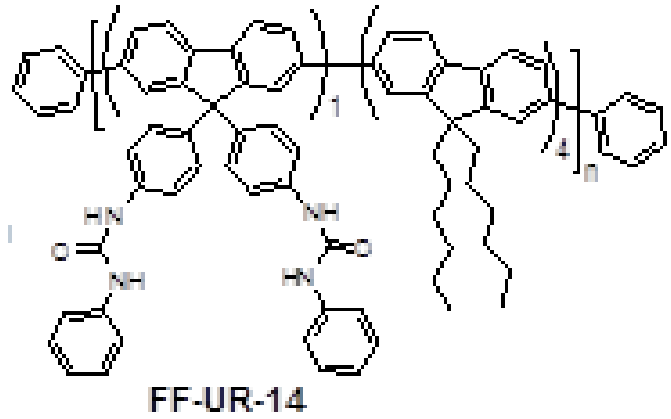


Figure 43 : Polymer for chloride detection bearing urea groups

5.5.5.3 Hardness monitoring: simultaneous detection of Ca^{2+} and Mg^{2+}

Monitoring hardness requires the capability to monitor jointly Ca^{2+} and Mg^{2+}. The $EDTA^{4-}$ anion is known for its capability to complex both these ions (Figure 44). A conjugated polymer was designed bearing pendant amino-carboxylate groups to mimic the complexing ability of $EDTA^{4-}$. (Figure 45).

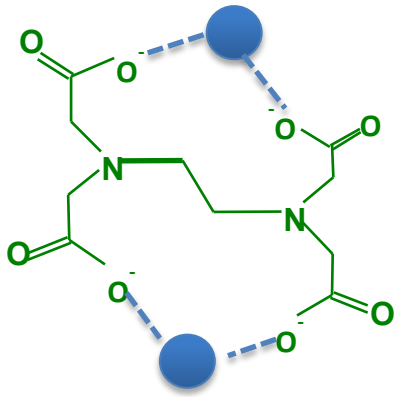


Figure 44 : [M2+(EDTA)]2- with M=Ca2+ or Mg2+ (one cation per pair of nitorigen atoms)

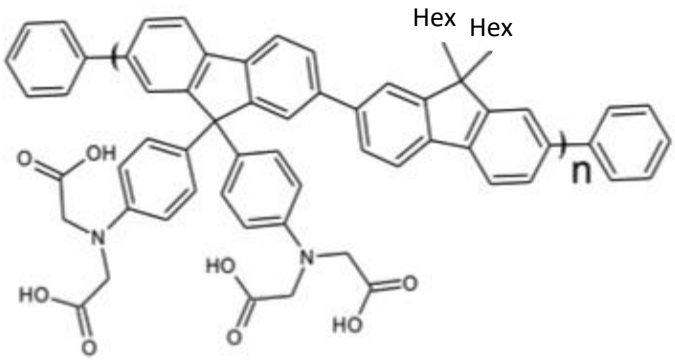


Figure 45 : Polymer for hardness detection bearing amino-caboxylate groups

5.5.5.4 Nitrate detection

The polymer for Nitrate detection will be described in D3.4.

5.5.6 Optimized transducer operation

The CNT sensors are biased with rectangular current wave (Figure 46) ranging between 0.5µA and 5µA, the preferred value for P2 process being 1µA. The duty cycle (t_{ON}/Period) is usually set to 10% for a frequency of 0.1Hz. Higher current and duty cycles have seemed to result in significant ageing (increase of resistance) during measurement.

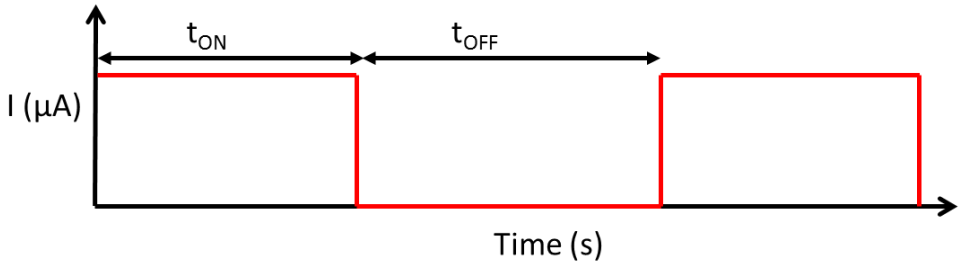


Figure 46 : Rectangular current biasing to operate the CNT sensors.

6 Energy harvesting and power management

6.1 Solution comparison

After having carried out preliminary test at Sense-City and SMAS (Almada), we have classified the viable solutions based on the ambient energy source availability. In case of drinking water network, the energy coming from the water flowrate is very variable and strongly depends on the deployment site and time. Table 8 summarize the strategy on the suitable energy harvesting technology.

Table 8 – Solution comparison per use case.

Use case	**Water Velocity** **< 0.2 m/s → Pw =4 mW***	**Water Velocity** **0.2-0.5 m/s → Pw= 62.5 mW***	**Water Velocity** **>0.5m/s → Pw > 62.5 mW**
Drinking water	WFEH is not efficient PV Panel**	WFEH based on turbine to be exploited Oscillating WFEH in not efficient	Oscillating WFEH is more efficient and not affected by blocking issues
Waste & Rain water	WFEH is not efficient PV Panel	Probably only PV panel	Oscillating WFEH is more efficient and not affected by blocking issues
* Mechanical power available from water calculated on 10 cm^2 flux section ** Estimated power of PV solar panel is aroung 100 mW on 10 cm^2			

As it can be seen in Figure 47, the average water speed of the drinking water network varies very much along a day. In particular, there is a minimum during the night, as expected, whereas, the max speed is reached around midday. The average water velocity ranges between 0.01 and 0.8 m/s at most.

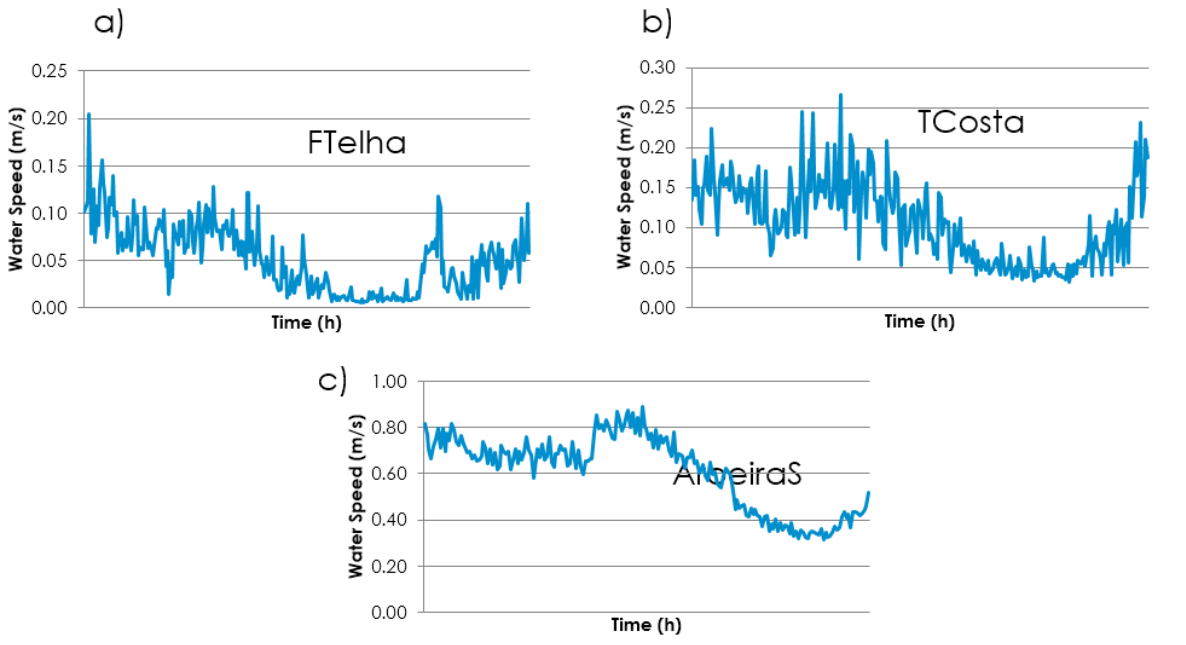


Figure 47: Water flux speed in different sites of the SMAS network (Alamada, Portugal).

At 0.2 m/s the available power is *P* = 4 mW calculated on a pipe section *S* = 10 cm^2. With such a constraint, we decided to choose a Water Flux Energy Harvester (WFEH) based on electromagnetic transduction instead of piezoelectric. The advantages of this technology are several:

- more than 10 times higher power density,
- easer design of the electromechanical coupling ,
- lower output voltage,
- lower optimal matching load,
- cheaper cost.

Among the different solutions, in order to achieve milli-Watts power level with on a section of 10 cm^2, an oscillating WFEH based on Von Karman vortex and Micro Savonius Turbine (MST) is proposed.

Table 9 – Solution comparison based on water average velocity.

Generator	**Water Velocity < 0.2 m/s → Pw =4 mW***	**Water Velocity 0.2-0.5 m/s → Pw= 62.5 mW***	**Water Velocity >0.5m/s → Pw > 62.5 mW**
PV Panel (10 cm^2)**	4.2 V – 22 mA (Thin Film) ** 1V – 100 mA (PolyCristalline Si)		
Piezo WFEH*	Power < 10 microW	0.12 Vrms - 0.16 mA Power ~20 microW @ 0.4 m/s	0.4 Vrms - 0.45 mA Power ~180 microW @ 0.8 m/s over Rl = 0.8 kOhm
Electromagnetic WFEH*	Power < 10 microW	< 1 mW because efficiency is strongly dependent on Reynolds number	Power ~ 50 mW @ 0.8 m/s *** Voltage and current depend on the design
Micro Savonius Turbine*	Power <1 mW	Power ~ 1-12 mW Voltage and current depending on the design	Power ~ 50 mW @ 0.8 m/s*** Voltage and current depend on the design
* Mechanical power available from water calculated on 10 cm^2 flux section ** Estimated power of PV solar panel is around 100 mW on 10 cm^2 . It depends on the product characteristics – (reported PowerFilm Co. model SP4.2-37) *** Estimated power with efficiency of 20 %			

In the deliverable D2.1 we targeted an energy consumption of the PNODE of **100 mWh/day** that is **360 Joules/day**. In order to achieve this budget, the necessary daily average power is **4 mW** which at a supply voltage of **1 V** correspond to **4 mA** average current. Note that these values are the averages on calculated on 24h, which means that the power consumption peak can be well above this threshold while the overall daily energy budget should not overcome **100 mWh**.

To achieve this objective for the 2nd run, new prototypes of oscillating EM WFEH and a Micro Savonius Turbine (MST) are designed as illustrated in the following paragraphs.

6.2 Integrated Energy Harvesting System

The energetic autonomy is a real challenge considering the levels of water velocity that strongly depend on the deployment site. The choice of a WFEH is only a viable technology in the case of drinkable water network. In the other cases: waste and rain water, the presence of solid residual makes only possible the use of photovoltaic panel in combination with high capacity battery. In the case of drinking water, both the PV panel and the WFEH can be integrated and linked to the PLC board, where the energy is collected into a conditioning and storage system based on supercap and battery. In principle, the WFEH

could be directly integrated in the same PNODE. However, to avoid the measurement interference with the sensing cap, we have chosen to use a second saddle clamp for the energy harvester, adopting however the same mechanical connection as the PNODE. The distance between water flux harvester and the sensing device can be adjusted.

Figure 48: Scheme of the integration of the energy harvesting system.

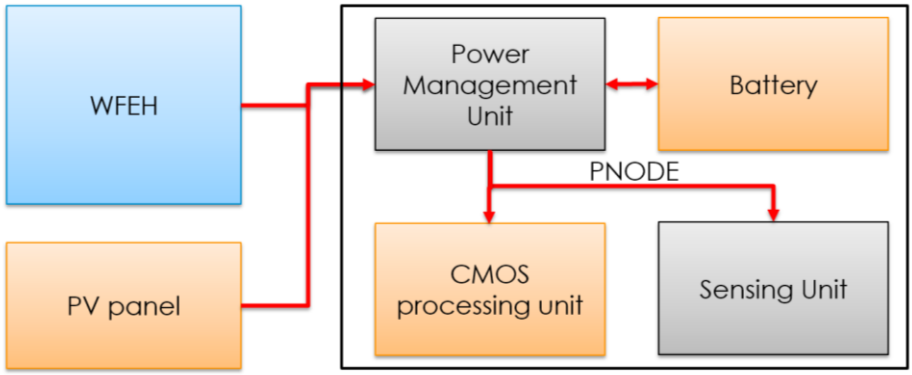


Figure 49: Block scheme of the system integration with energy flux.

Figure 49 shows the block scheme of the system integration of EH+PNODE with energy flux direction. The type of PV panel and the capsule integration with the WFEH is discussed in the deliverable D5.1.

6.3 Water Flux Energy Harvester (WFEH)

6.3.1 Oscillating Electromagnetic WFEH

The mechanical principle of the oscillating WFEH is the one used in the 1st energy harvester version based on a cantilever piezoelectric generator as explained in D5.1. As shown in Figure 50, the harmonic lift force is produced by Von Karman vortex along the axis transversal to the flowrate direction around the moving cylinder. The best operating region for the WFEH occurs when the Strouhal number is around 0.18 and Re = 1.6×10^5. This condition is verified for velocity range around 1 m/s depending on the impact section of the device.

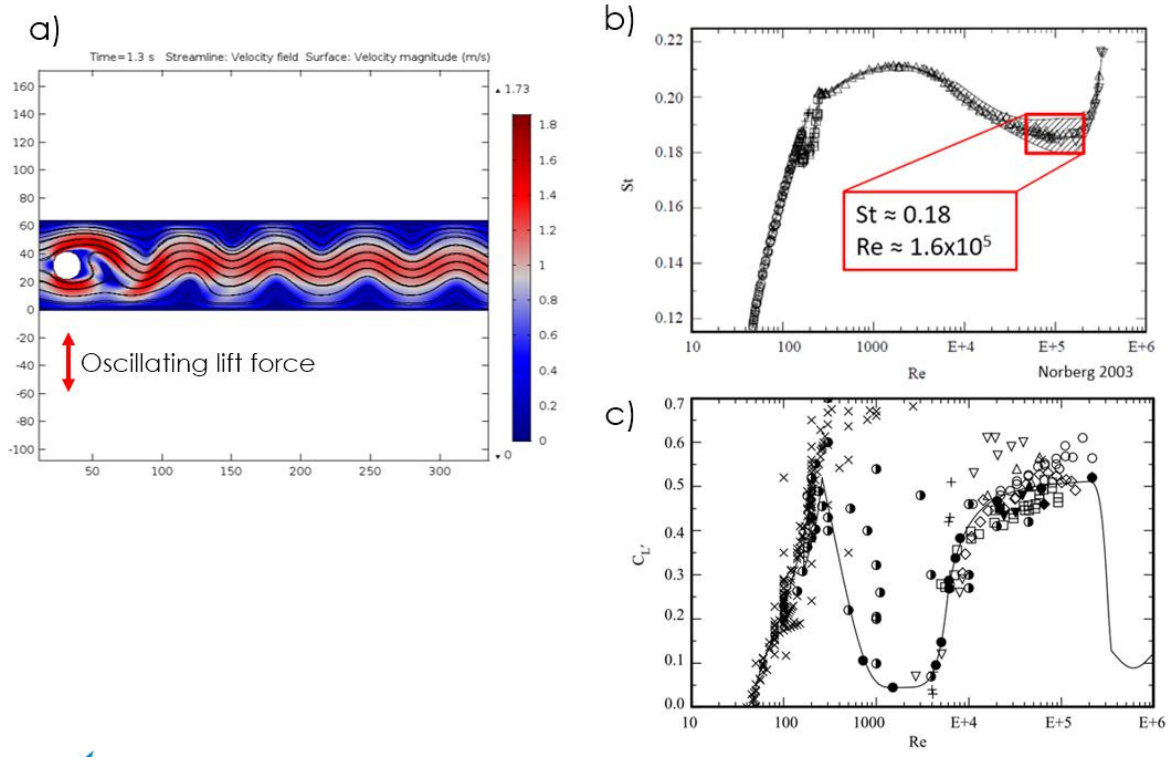


Figure 50: a) Simulation of the lift force induced by Von Karman vortex around a cylinder. c) Efficiency C_L correlated to b) the Strouhal number vs Reynolds number[4].

In the SMAS (Almada) network the velocity ranges between 0.1-0.8 m/s, but most of the time is well below 0.5 m/s. This aspect constitutes a challenge in the capability of small harvester to capture energy at very low speed. In fact, the lift force frequency is derived from the Strouhal number as $f_s = St\ v\ /D$, where v and D are the water velocity and the cylinder linear dimension, and the Reynolds number is calculated as $Re = \rho v D/\mu$, where ρ and μ are the density and dynamic viscosity of the water. Thus, the energy harvester should operate in a very low frequency range f_s = 1 – 8 Hz and with a turbulence regime of Re = 2 x 10^3 - 1.8 x 10^4 which is lower than the optimal region stated above. As a consequence, the oscillating WFEH must work at very low frequency, whereas the Micro Savonius Turbine will have difficulty to self-start below a threshold of 0.2 m/s.

In order to address this issue, we design new nonlinear and more efficient concept of WFEH. Regarding the oscillating generator, the main difference with respect to the 1st piezoelectric version harvester lies in the transduction technique. The 2nd version here is based on magnetic induction generated by the change of the magnetic flux linkage through an iron circuit. In details, when the cylinder oscillates, a magnetic switch changes the direction of the magnetic flux linked to the solenoid. Hence, the variation of the magnetic flux induces a current and voltage potential directly proportional to the angular velocity of the mass.

Figure 51 shows the CAD design of the generator adapted to the same mechanical housing of the PNODE capsule that is illustrated in D5.1 and D2.1. The magnetic field is generated by An N42 grade NdFeB permanent magnet of 10 x 10 x 10 mm^3. Three iron foils carry the magnetic flux with alternate

[4] C. Norberg, “Fluctuating lift on a circular cylinder: Review and new measurements,” J. Fluids Struct., vol. 17, no. 1, pp. 57–96, 2003.

polarity (Nord-South-North) and couples with two iron foils that represent the iron core expansions of the coil (with around 2000 loops), once N-S and once S-N in turns. An important characteristic of this new concept is implemented in virtue of the magnetic switch principle: the dynamic bistability of the oscillating mass. This feature is demonstrated to the advantageous because of the wider response of nonlinear vibrational harvester in the frequency domain[5]. The output voltage and electrical power delivered to the load R_l can be approximated in the following formula

$$V_{out} = Bl\omega R \quad (1)$$

$$P = \frac{V_{rms}^2}{R_l} \quad (2)$$

Where ω, l, R and B represent the angular velocity, the total length of the wire coil, the radius of the rotating cylinder and the maximum magnetic field felt by the coil.

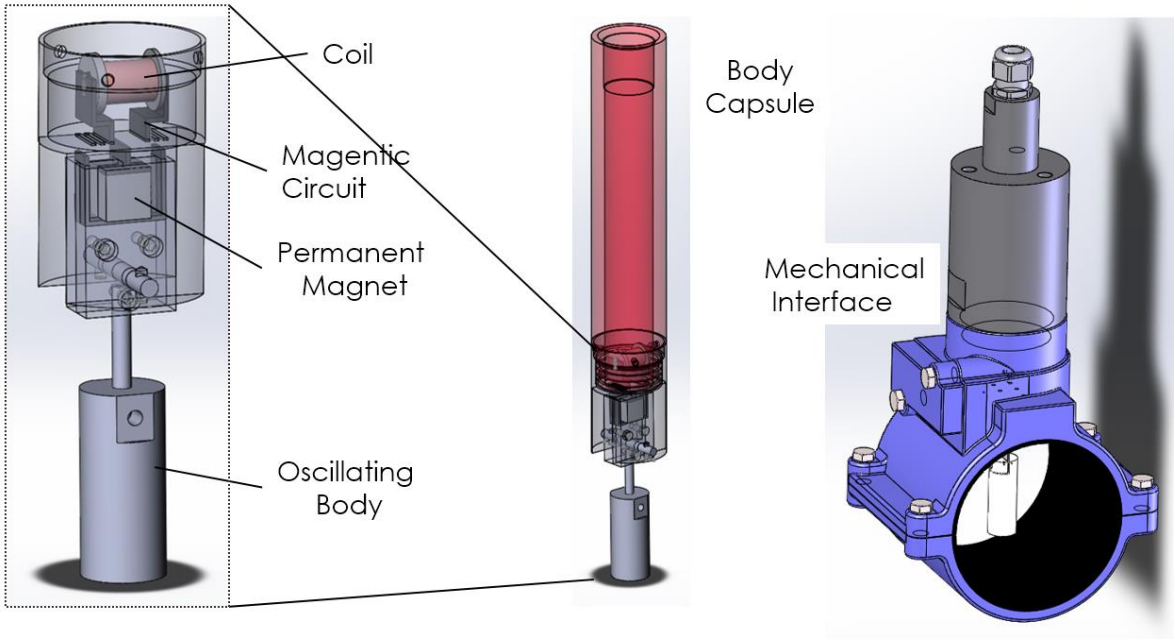


Figure 51: Design of the oscillating WFEH (left) with mechanical connection (right).

[5] F. Cottone, H. Vocca, and L. Gammaitoni, "Nonlinear Energy Harvesting," Phys. Rev. Lett., vol. 102, no. 8, p. 80601, Feb. 2009.

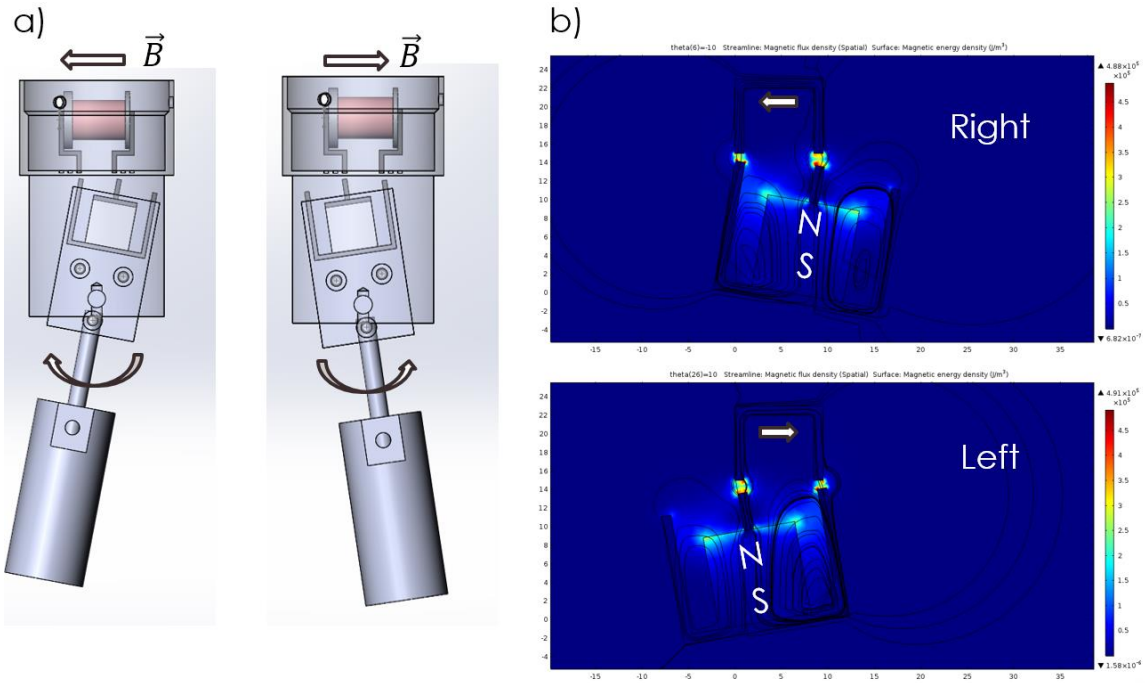


Figure 52: a) Magnetic circuit switch with positions of the oscillating WFEH, b) Finite Element Analysis of the magnetic flux for the right and left stability point.

Figure 52 a) illustrate the magnetic switch principle with oscillating mass stability positions (left and right) that correspond to the maximum magnetic flux linked to the coil. Figure 52 b) shows Finite Element Analysis of the magnetic flux by sweeping the rotational angle. This calculation provides the stability points and the magneto-static potential illustrated in Figure 53.

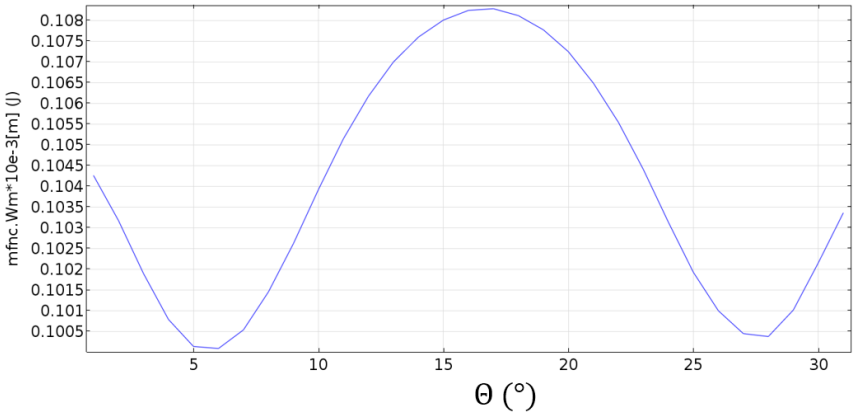


Figure 53: Magneto static potential energy Vs rotational angle of the oscillating body.

6.3.2 Micro Savonius Turbine

A micro hydro turbine is also designed to compare with oscillating WFEH in terms of performance. Given the water speed range 0.1 – 0.8 m/s, the best solution for a Tip Speed Ratio λ=1, among different geometries, is the a Savonius type. A Micro Savonius Turbine (MST) provide good value of efficiency, C_p, at low water speed with respect to other types. Figure 55 shows the micro hydro turbine, which measures 35 mm of height by 24 mm of diameter, almost the same size of the oscillating WFEH. The

estimated electrical power is between 5 and 10 mW, in the water speed range of 0.5 – 0.7 m/s with an efficiency around C_p = 0.15 (that is 15 %).

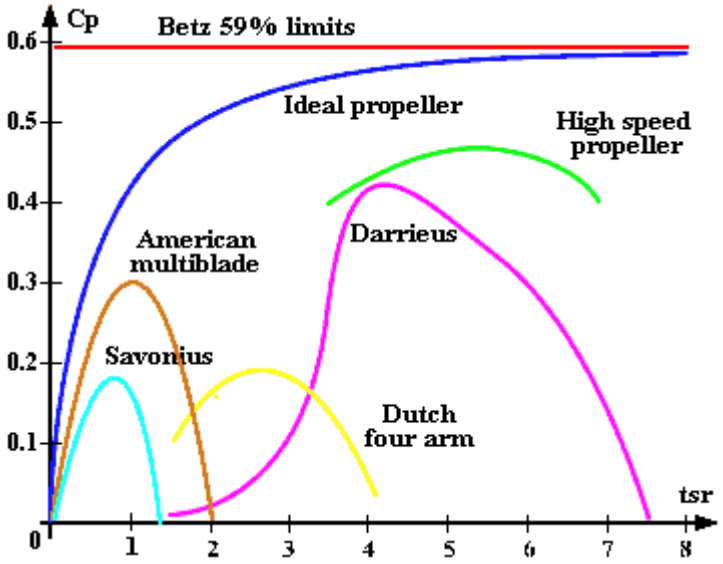


Figure 54: Efficiency C_p coefficient Vs Tip Speed Ratio (TSR) for different Turbine design (Menet).

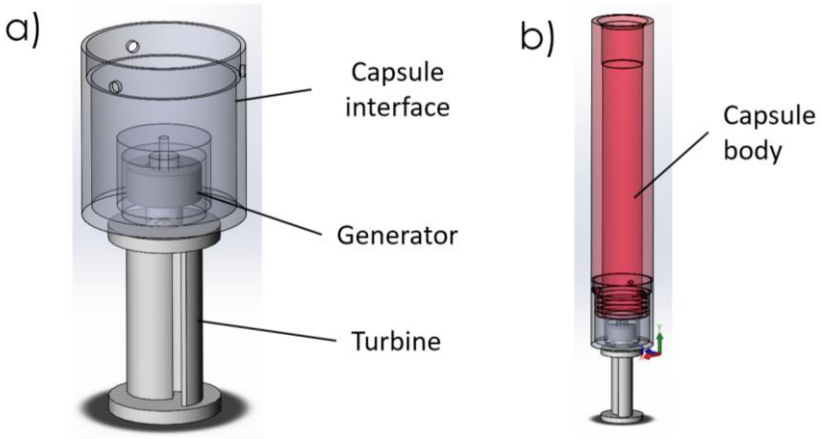


Figure 55: Micro Savonius Turbine a) with capsule interface support b).

7 Software

7.1 Integration of Embedded Operational Software

7.1.1 Reminder: Description of states + state machine diagram

Six (6) different modes of operation for the PNODE are identified:

1. **Regular Measurement mode**: regular measurements are taken from primary sensors.
2. **Alert Measurement mode**: when in alert mode, measurements are taken from primary sensors with increased frequency and data is prepared to be sent more frequently. The Alert state comprises 2 substates, i.e. Alert and Alarm, which have different Monitoring Profiles and 1 additional substate, i.e. Extrapolation.
    - Alert substate is evoked when at least one measurement is between the alert and the alarm thresholds.
    - Alarm substate is evoked when at least one measurement passes the alarm threshold.
    - Extrapolation substate is evoked when there is need for predicting the current or future value e.g. due to malfunction or irregular (out of range) measurement, large variation or large noise or unexpected rate of change, the latter cases leading to more smart processing and need to communicate with WMS.
3. **Control/signalling mode**: when in control/signalling mode, the PNODE receives configuration messages from the WMS comprising e.g. parameterization.
4. **Communication mode**: in this mode, the PNODE is transmitting data (keep alive signals and sensing data).
5. **Sleep mode**: the device enters into this mode every time it does not have anything to do. No measurements/processing/transmission, but waiting for control commands. This state is essential to extend the autonomy.
6. **Panic state**: running out of energy “very soon”. The device must proceed with data transmission and transition to Sleep mode.

Further details can be found in D2.1.

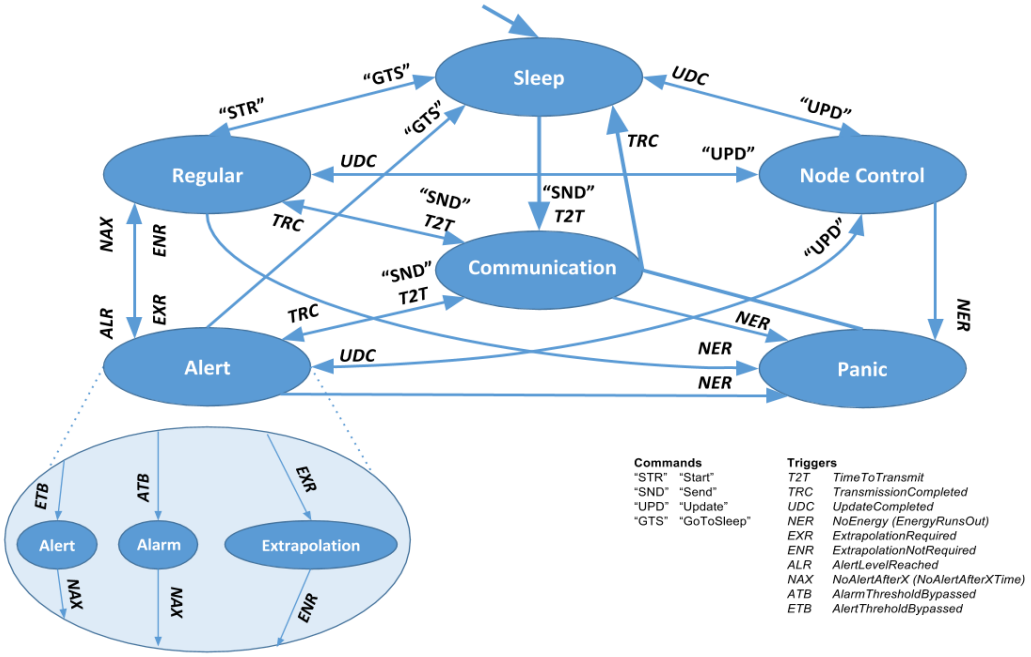


Figure 56 PNODE Embedded Software State Machine

Table 10 State Transmission Table

Modes of operation	Command or event and conditions met	Next modes of operation	Output (action the node must carry out) and Functions called
Sleep	"Start" **start == true**	Regular	Activate primary sensors **ActivatePrimarySensors(Sensors, index)**
Regular	"GoToSleep" **sleeping == true**	Sleep	Deactivate primary sensors **DeactivatePrimarySensors(Sensors, index)** Put the sensor in sleep mode
Regular	TimeToTransmit **timeToTransmit == true**	Communication	Keep alive signals Data sent to WMS **DataToSCADA(Sensor, timeToTransmitSensor, index)**
Regular	AlertLevelReached **alertReached == true**	Alert	Increase measurement frequency **IncreaseMeasurementFrequency (Sensor, index)** Change TimeToTransmit (communication periodicity) May activate secondary sensors if requested by use case and/or possible with energy budget **ActivateSecondarySensors(Sensors , index)**
Regular	ExtrapolationRequired **casePredict == true**	Alert	May predict next expected measurements **DoubleExpon(a, ,b ,c ,d ,e ,f)** May/Must go to Communication mode to send warning **DataToSCADA(Sensor, timeToTransmitSensor, index)**
Alert	ExtrapolationNotRequired	Regular	-
Alert	NoAlertAfterX	Regular	Decrease measurement frequency

			DecreaseMeasurementFrequency (Sensors, index) Deactivate secondary sensors in case of previous activation **DeactivateSecondarySensors(Sensors, index)**
Alert	"GoToSleep" **sleeping == true**	Sleep	Deactivate primary sensors **DeactivatePrimarySensors(Sensors, index)** Deactivate secondary sensors in case of previous activation **DeactivateSecondarySensors(Sensors, index)**
Alert	TimeToTransmit **timeToTransmit == true**	Communication	Data sent to WMS immediately **DataToSCADA(Sensor, timeToTransmitSensor, index)**
Node control	UpdateCompleted **updateCompleted == true**	Previous state (Sleep, Regular, Alert)	Return to previous state
Communication	TransmissionCompleted transmissionCompleted == true	Previous state (Sleep, Regular, Alert)	Return to previous state
Communication	TransmissionCompleted and previous state is Panic **transmissionCompleted == true && State.previous_state == panic**	Sleep	Go to Sleep to charge
Sleep Regular Alert	"Update" **updating == true**	Node control	Over the air parameterization (define threshold, alert levels) Over the air programming
Sleep Regular Alert	"Send" **sending == true**	Communication	Data sent to WMS immediately **DataToSCADA(Sensor, timeToTransmitSensor, index)**
Regular Alert Communication Node control	NoEnergy (Energy runs out) **noEnergy == true**	Panic	Go to Communication mode to send warning (and data) to WMS **DataToSCADA(Sensor, timeToTransmitSensor, index)**

The functions definition in the Output column are given in section 7.1.1.2 and 7.2.

7.1.2 Functions definitions

Below, we present the definitions of the more important functions that are being used by the PROTEUS operational software, updated from the D4.1 section 3.5. These functions are the main specifying the smart behaviour of the PNode and the ones that will be provided by the Analog Front End API and/or the Communication API in the second run. Alongside the definitions, we included the type of each variable, information about that variable, and the return type – if exists- of the function.

```
/* Struct of arrays containing the information of every sensor */
struct Parameter
{
        char Name[25];
        int Criticality;
        uint8_t Minimum;
        float Maximum;
        float Current;
        float MinAlarm;
        float MinAlert;
        float MaxAlert;
        float MaxAlarm;
        float MeasurementFrequency;
        float TimeToTransmit;
};
/*end of struct */



/*****************************************************************/
static void checkStates();
//This is the state machine implementation on the PNode. It is responsible for the
//transitions between the various states that have been defined in D2.1.

/*****************************************************************/
/*
*@param Sensor is an array that holds the information of each parameter
*@param timeToTransmiSensor is an array which updates when a transmission has to
be done for a parameter
*@param index is the index of the parameter we wish to send the data
*/
static void DataToSCADA (Parameter *Sensor, uint8_t *timeToTransmitSensor, uint8_t
index);
//Transmits to WMS the information of the parameter we are interested to.

/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to activate the primary sensors
*/
static void ActivatePrimarySensors(Parameter *Sensor, uint8_t index);
//it receives the index of the parameter that we want to activate its primary //sensors, its
information, and for the time being it only prints a message.
```

```
/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to activate the primary sensors
*/
static void ActivateSecondarySensors(Parameter *Sensor, uint8_t index);
//Same as above, but for the secondary sensors.

/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to increase the measurement frequency
* @return updates the time that the next measurement should be sampled
*/
static float IncreaseMeasurementFrequency (Parameter *Sensor, uint8_t index);
//This function receives the index of the parameter that we want to increase its //measurement frequency, its information, and
//increases the measurement frequency of that parameter accordingly to its //criticality.


/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to increase the measurement frequency
* @return updates the time that the next measurement should be sampled
*/
static float DecreaseMeasurementFrequency (Parameter *Sensor, uint8_t index);
//This function receives the index of the parameter that we want to decrease its //measurement frequency, its information, and
//decreases the measurement frequency of that parameter accordingly to its //criticality.


/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to activate the primary sensors
*/
static void DeactivatePrimarySensors(Parameter *Sensor, uint8_t index);
//This function receives the index of the parameter that we want to deactivate its //primary sensors, its information, and for the time being
//it prints a message.

/*****************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to activate the primary sensors
*/
static void DeactivateSecondarySensors(Parameter *Sensor, uint8_t index);
```

```
//This function receives the index of the parameter that we want to deactivate its
//secondary sensors, its information, and for the time being
//it prints a message.

/*********************************************************************/
/* @param index is the index of the parameter that we are currently checking its flags
* @param SensorValues array that holds the information of each parameter
* @param COUNTALERTS array that stores the amount of consecutive alerts of every
critial parameter
* @param COUNTALERTSNON array that stores the amount of consecutive alerts of
every non-critical parameter
* @param COUNTALARMS array that stores the amount of consecutive alarms of every
critial parameter
* @param COUNTALARMSNON array that stores the amount of consecutive alarms of
every non-critical parameter
*/
static void check_flags(uint8_t index, Parameter *Sensor, uint8_t *COUNTALERTS,
uint8_t *COUNTALERTSNON, uint8_t *COUNTALARMS, uint8_t *COUNTALARMSNON);
//This function checks whether or not a min/max - alert/alarm threshold has been //passed
and updates the flags accordingly.
//Also it checks whether or not the extrapolation flag has been triggered. Finally, it
//stores the amount of consecutive alarms/alerts that may have happened.


/*********************************************************************/
/*
* @param Sensor is an array that holds the information of each parameter
* @param index is the index of the parameter we wish to read samples from the ADC
*/
static void ReadValues(uint8_t index, Parameter *Sensor);
//This function receives the index of the parameter that we want to activate its //primary
sensors, its information proceeds to update the current
//value of this parameter.


/*********************************************************************/
```

7.1.3 Description of operational software at interface/system level

The integrated system allows the capture of various external and internal interrupts, which enable special functionalities, like the acceptance of Modbus messages. Furthermore, it allows the communication with other devices or chips that are present on the V1.2 board using SPI and UART protocols.
The SPI protocol will be used for the communication with the external FLASH memory; the external memory will have to ask for the permission of the oMSP before sending back information that was asked. This query from the external memory will be understood by the oMSP with the help of an interrupt on a dedicated pin.
Finally, a UART protocol will be used to give commands and receive values from the AFE.

7.1.4 Brief statements on programming language and tools

The language used for programming the state machine on the MSP430FR5969 board is C. The IDE that was used initially was Energia, an IDE that let us rapidly program a platform using Arduino like commands and libraries. The code was then transferred to Texas Instruments' Code Composer Studio to allow us better debugging and monitoring of the power consumption. The MSP430 board can be programmed with one of the above IDEs and a USB cable.

7.1.5 Interrupts Management

7.1.5.1 List of interrupts that may affect our operation

From highest processing required, to lowest

i. UART RX interrupt: have we received an incoming Modbus message?
ii. SPI interrupt: the slave wants to send us something
iii. Px.x interrupt: if this pin received a predefined logical state (0 or 1), it means that we are running low on energy. It will interrupt the code execution and send us to panic mode
iv. Timer interrupt: every one second, add a second to the real-time clock

7.1.5.2 Strategy on how we manage them

Having got the MSP replying to every Modbus message frequently (e.g. more than 5 times in a minute, is an extremely energy-consuming process. The proposed management is to add an UART interrupt to receive the incoming messages. The interrupt service routine (ISR) will decide when to send back to the Modbus master the reply.

Another ISR will be added for the SPI protocol. When we ask for data retrieval from the external FLASH, the slave will inform us that it is ready to send us by triggering an interrupt on a dedicated pin.

Also, a dedicated pin can be used to inform us that we are running low on energy. This ISR can be triggered by a logical state (0 or 1) and drive the operational software to panic state and then to sleep state.

7.2 Embedded Predictive Software

This software should address the ability of PROTEUS system to anticipate the occurrence of a critical event. At this stage, we consider the ability of the system to predict the next instance(s) of the most critical sensing parameters for the use case that the system operates within, so as to be used for the identification of a future alert/alarm under normal or exceptional situations or for compensating for a current non-proper reading. Exceptional situation can be the energy starvation or a rapidly evolving critical event. Non-proper reading may be a noisy or out of range measurement or even a failure to measure.

The approach is to develop an algorithm based on time series analysis. This method was chosen, because the frequency of the sampling of the data we possess was constant (two minutes and 30 seconds), thus fulfilling the definition of time series.

A time series is defined as a series of data points listed in time order. Most commonly, a time series is a sequence taken at successive equally spaced points in time. Thus, it is a sequence of discrete-time data [8].

For time series forecasting, two different methods can be used to train the data and make predictions. The first method is called "**moving average**" and the second "exponential smoothing". Whereas in the moving average method, the past observations are weighted equally, exponential window functions assign exponentially decreasing weights over time [9].

When using the moving average algorithm, a short statistical analysis takes place before forecasting. We must first find the baseline, the trending and the seasonality of our data before making predictions.

For the exponential smoothing method, there were used 2 different algorithms. The **simple exponential smoothing** algorithm and the **double exponential smoothing**. The simple exponential smoothing is fast and it only needs the current measurement and the previous forecast in order to make a prediction for the next value. The double exponential smoothing is also fast, it needs a quick statistical analysis in order to find the best estimate and the smoothed value at time t, using the current measurement and the previous forecast. The triple exponential smoothing is a bit slower because it needs lots of data in order to train and make predictions, but it has more capabilities than the 2 other smoothing algorithms; it can cast predictions for the entire next period after our last sample. To do so though, we have to "feed" the algorithm with at least 2 past periods of data in order to initialize.

For the **simple exponential smoothing** algorithm, we only need the current value, the previous forecast and a coefficient (alpha) between 0 and 1. The optimal value for the coefficient can be found using various optimization techniques.

For the **double exponential smoothing** algorithm, we need two coefficients (alpha and beta), where their values are within the [0,1] range.

The algorithm that was selected for deployment on an embedded system is the Double exponential smoothing, for the following reasons:

- **Extremely lightweight algorithm**: only 1052 bytes of FLASH and 36 bytes of RAM required.
- **Faster execution time**: Double exponential smoothing requires 512 μsec for execution.
- Double exponential does **not depend on an array of past measurements**, it only needs the previous measurement for making predictions.
- **It gives very good results**, with Mean Absolute Percentage Error varied from 93.35% to 100%.

Mean Absolute Percentage Error is given by $MAPE = \frac{100}{n} \sum_{t=1}^{n} \left| \frac{A_t - F_t}{A_t} \right|$, where A_t is the actual value and F_t is the predicted value. The algorithm was trained on small sub-sets which were pulled out of a larger

data set. If the small data set has a length L, we predict the L+1 value and compare it to the actual sample from the larger data set.

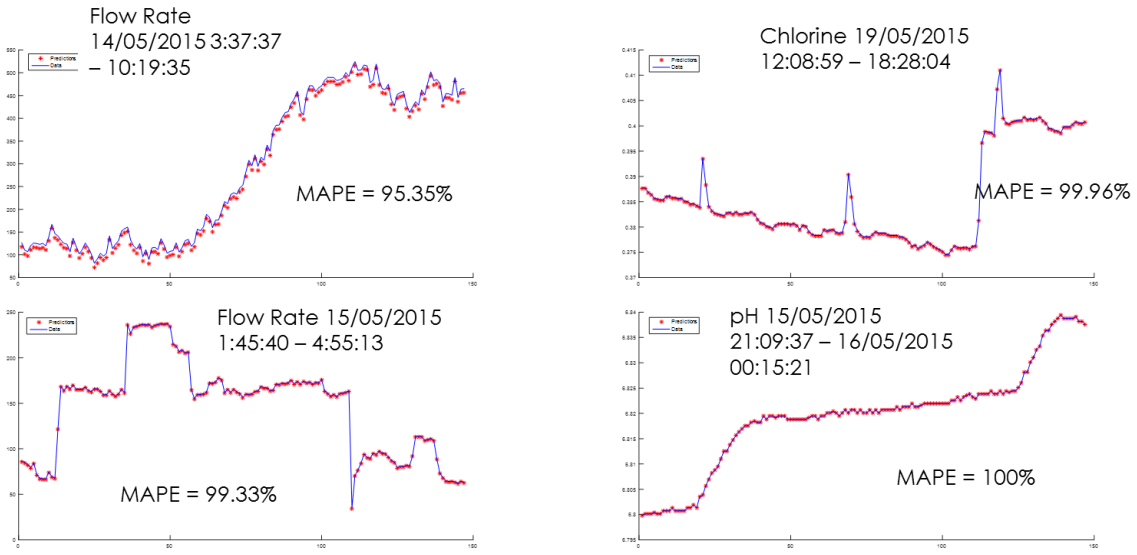


Figure 57 Double exponential smoothing algorithm results

7.3 WMS Predictive Software

The following technique, namely the **triple exponential smoothing**, was tested on the WMS-based software. For the triple exponential smoothing, we need to know the period of the waveform of the time series for our algorithm (recall 'L' from the formula which was presented earlier). In order to find it and use it, we used a Fast Fourier Transform on our data sets, so we could find the power spectral density of the waveform. The maximum value of the power spectral density corresponds to the fundamental frequency of the data set, thus by using:

$$T_{fundamenental} = \frac{1}{f_{fundamental}}$$

We found the period of the data set and used it on our algorithm.

The algorithm that was selected for deployment on the WMS system is the Triple exponential smoothing, for the following reasons:

- **Faster training** than neural networks: On average a Neural Network requires 8-10 seconds for single training and multiple trainings have to take place to achieve an unbiased training. Triple exponential requires **less than half a second** for its training (tested with SMAS data as well as Sense-City data)
- **Triple exponential can predict values up to an entire period ahead**. With the neural networks we could only predict the next few measurements before the values started saturating at the average value of the samples. Triple exponential requires 2 periods of data for its training and initialization. The period of the data set can be found with FFT, by finding the frequency where the power spectral density is max. Thus period = 1 / frequency. **Period varied from 1 day to 2 days**
- **It gives very good results**, given its long term capabilities, with Mean Absolute Percentage Error varied from 81.97 % to 98.54%.

The algorithm was applied to parts of the data-set to check if it could foresee the values that we already have. The amount of predictions was set to be equal to half the period of the data-set.

In order to test if the predictions can follow the actual data, the red line should be close to the cyan line.

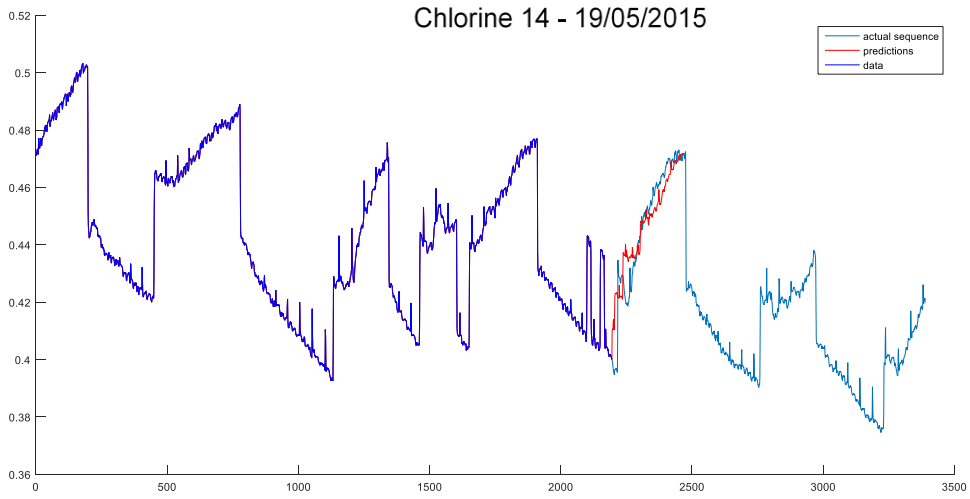


Figure 58 MAPE = 90.36 %

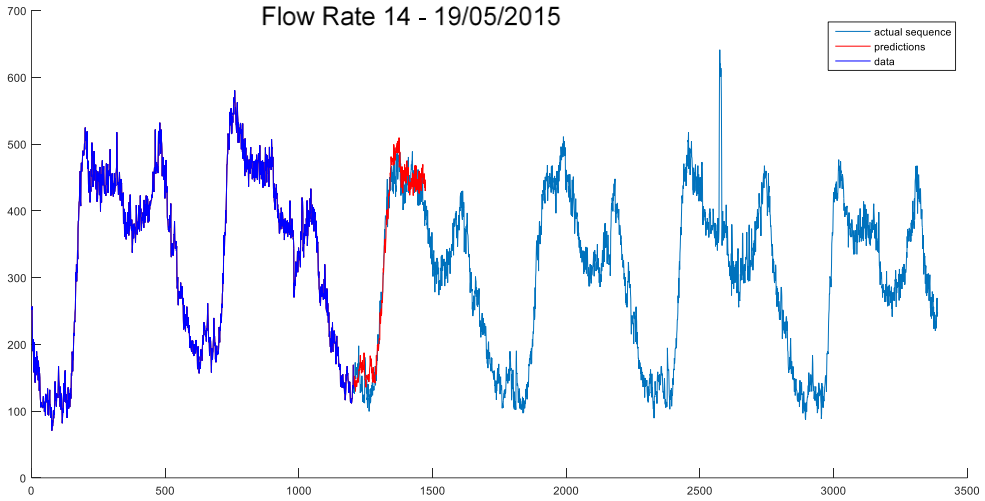
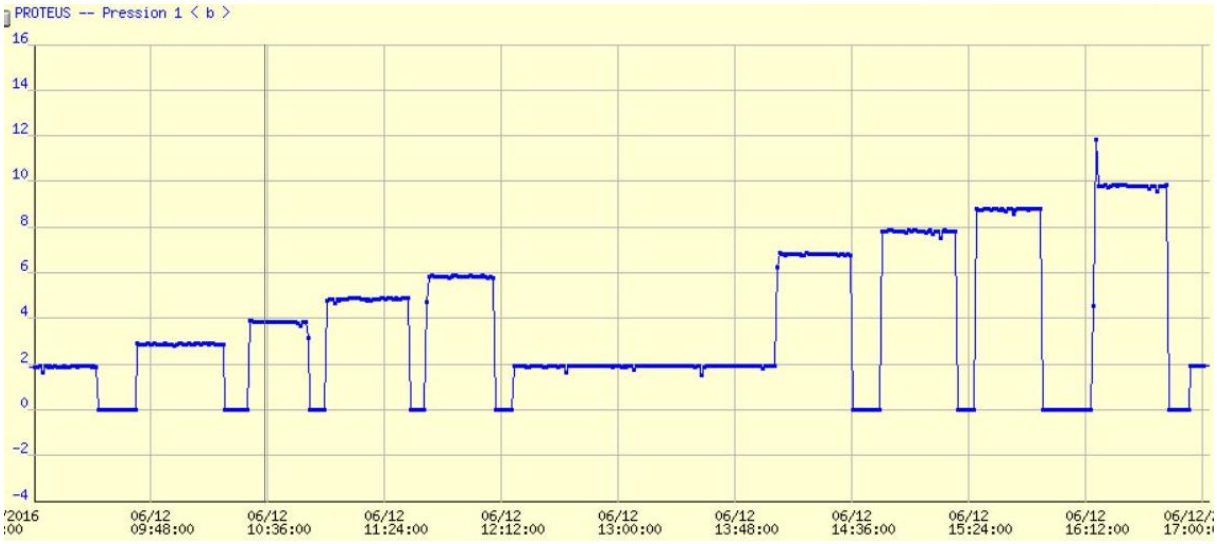


Figure 59: MAPE = 98.45 %

8 Housing

8.1 Summary of the mechanical tests in Sense-city loop :

The housing of PNODE version 1, based on two mechanical parts, sensor cap and node housing have been evaluated in Sense-city loop configuration in the pressure range of 2 to 10 bars.

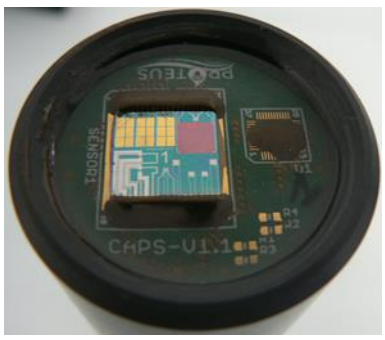
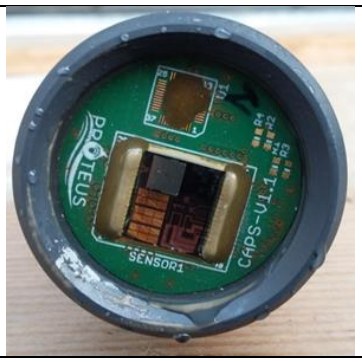


Graphical view of the pressure step during the test in Sense-city drinking water loop

The complete mechanical system have successfully resisted in these in-pipe conditions (pressure and flowrate 20m^3/h). Consequently, the design of cylindrical node housing and the watertight assembly with the sensor cap, based on two O-rings, will not change for the next version.

8.2 Behaviour of the sensor cap assembly

Considering the sensor cap, the trials in Sense-city drinking water loop highlighted a weak point. The globtop coating on the two opposite side of the sensor chip moved and did not significantly cover the pads aera (see pictures below).

		
Final step of assembly and coating	After 44 days in water into the loop (18th october to 6th december)	After pressure test, 2 to 10 bars

8.3 Optimized resist choice and curing profile

In order to eliminate this unexpected behaviour, glob top resin lifted up, alternative strategies of coating of the cross-side of the sensor cap have been identified. The possible improvements are listed below.

1/ selection of glob top resin:

Among the wide range of resins, our first choice of bi-component epoxy resin supplied by Epotek (H70E-4) have been re-examined from physical properties standpoint. While the stability of resin in water flow remains a main objective, we also focus on the adhesion property on the top layer of sensor chip (Al_2O_3 and gold) and the compatibility with a flexible substrate (printed circuit board submitted to pressure). Consequently, epoxy resins from alternative suppliers and silicone elastomer are under investigation.

2/ Optimization of the coating process:

The choice of resin is not the only way to increase the reliability of the assembly around the sensor chip. The parameters of coating process could be optimized. In order to minimize stress, a low cure temperature could be managed but will result in slow cure and low crosslink density. The drawback in such case, is that they may not yield the desired optimal performance. Ramped or stepped cure will be investigated as a good compromise between a high and a low temperature. This often provides a balance between lower stress as the cross-linked structure is slowly locked and a higher overall level of crosslinking as higher temperature level are ultimately achieved.

9 Conclusions

This report provides the operative design specifications that guide the realization of the second version of the PNODE. With respect to the first version, specified in D2.1, the work of D2.2 addresses the main limitations encountered in first assembled prototype, throughout the fabrication and test carried out in laboratory and in the Sense-City platform (D5.1 and D5.2). These limitations mainly regard the difficult integration of each building block both at hardware and software level, the acquisition of the sensing information and the effective powering for each use-case. Besides, each sub-system has been improved based on the new requirements observed from the validation test.

To this aim, the D2.2 provides the following main changes with respect to the previous design (D2.1):

- **CMOS chip**: successful low power integration of the electronics in a single CMOS chip with improved DC-DC converter for power management and wireless capability. Optimization of the analog front end and digital processing unit in addition to the signal acquisition and elaboration.

- **MEMS sensors:** full co-integration of all PROTEUS sensors (up to 16) on a single monolithic silicon chip: with chemical sensor based on CNT along with physical ones.

- **Sensor cap PCB:** full integration of CNT array up to sensor caps level (fully packaged) with MEMS and CMOS, in a relatively low cost process. Optimization of the protective coating

- **Energy Harvester:** novel design of the water flux energy harvester based on Von Karman vortex with electromagnetic transduction. This approach bring the advantages of higher power density and lower cost. In addition, a Micro Savonius Turbine is proposed to work well at lower water speed, 0.2 – 0.5 m/s.

- **Software:** integration of embedded operational and predictive software. Cognitive processing are performed inside the PNODE, analysis of field situations (sensing measurement) and operational parameters (memory, power availability). Software available on the same chip as used in PNODE with mock up data.

- **Housing:** selection of new glob top resin and optimization of the protective coating of the sensor cap.

These improvements will serve to complement and conclude the WP2. The outcome of this work will provide the roadmap for the fabrication, integration and testing in real environment of the final version of the PNODE.